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EXPERIMENTAL INVESTIGATION FOR DETERMINING HEALTH STATE OF GAN TRANSISTORS

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Abstract-This paper explores the feasibility of using surface measurable parameters to track degradation of Gallium Nitride (GaN) field effect transistor (FET) installed and operational on a circuit board. To validate the premise, a preliminary investigation, focused on magnetic field of the bulk of the transistor as well as drain-source voltage and dynamic on-state resistance, is performed. A sustained 57% increase in on-state resistance of stressed transistors over their unstressed counterparts in a DC-DC converter circuit in the absence of stressing voltage, indicated irreversible change in material properties of the constituent semiconductor. This change is also manifested in the positive shift of magnetic field strength. The magnetic field of the bulk thus are found to be a viable degradation marker and so are permittivity and permeability with equal possibility, which, with further in-depth study, could lead to a robust model for real-time tracking of degradation in circuit-active GaN FETs

Keywords-GaN FET, Reliability, Magnetic field

I. INTRODUCTION

Sudden failure of semiconductor devices is highly undesirable and yet common in a range of power devices today. Overvoltage and other electrical stress conditions may occur during device operation and damage the device or significantly alter the life expectancy of such devices. These unexpected failures in semiconductor devices similarly occur in GaN-based power FETs as well. Some of the degradation and failure mechanisms unique to GaN-based FETs are discussed in detail in [1] and [2]. The latent failures of these devices may be critical when they manifest in certain application environments such as automobiles and space exploration systems. As a means for statistical reliability estimates, accelerated stress testing are well studied in the literature, in which reference [3] presents models obtained for semiconductor failure rate using an acceleration factor while reference [4] introduces a model for capacitor monitoring to predict failures. The estimating models typically involve the tests performed on a sample of devices with extrapolations to possible field application failure rates. For the failure rate of semiconductor devices in field service, data generated from operating life test sampling is the principal method used by the industry in estimating the failure rate. While these estimates are useful, they do not account for stress conditions that may occur during device operation. Further, if the objective is detection of overstressed state of a GaN transistor which is already installed on a board and under operation, much of today's diagnostic methods are inapplicable. Our research focus is to explore ways to fulfill the said objective by relating the internal property change such as on-state resistance with the externally measurable parameters such as magnetic field strength.

This paper presents a preliminary experimental investigation of external parameters of GaN FET exposed to normal and stressed conditions with focus on magnetic field, drain-source voltage (VDS) and dynamic on-state resistance (RDS-ON). The conjecture is that the channel current magnetic field will be modified by the bulk under degraded condition and that the magnetic field associated with charge transport across the bulk will be changed due to temperature gradient after stress. Therefore, any changes in the two dimensional electron gas (DEG) and bulk charge transport due to degradation (or stress) will manifest in the magnetic field strength shift.

On-state resistance RDS-ON is known to be failure precursor in MOSFETs [5, 6]. Reference [7] outlines a method for RDS-ON online monitoring in GaN FETs. A distinction is made between conduction and dynamic RDS-ON changes and their significance in health monitoring for the GaN. Conduction RDS-ON is identified

as a degradation-sensitive parameter while the dynamic RDS-ON changes are perceived to be insignificant. This view on dynamic RDS-ON may not be exact since charge trapping causes dynamic RDS-ON and can behave differently in a device, operational in a circuit. A recent work reports the impact on dynamic RDS-ON in continuously operating converters with 35.9% increase over the DC value [8]. We conjecture that the known faults of GaN FET (traps, self-heating etc.) may, generally, behave differently in active circuits, manifesting therefore differently than previously perceived in surface measurable parameters reflecting the internal material properties of the transistor bulk (heterostructure of GaN and substrate). Assessing parameters over the range of normal and stressed operating condition may yield a qualitative evaluation of the health status of the transistor.

To validate our conjecture we conduct a preliminary experimental investigation of surface parameters of the GaN FET after exposing it to normal and stressed conditions with focus on the following parameters: magnetic field strength, drain-source voltage, and dynamic on-state resistance.

II. EXPERIMENT SET UP

For our experimental investigation, a DC-DC converter board with two GaN FETs from Texas Instruments (TI) is selected:LM5113 evaluation board. The LM5113 evaluation board is made for TI's LM5113 driver chip for GaN FETs, but our main purpose of the board is on the GaN FETs themselves. As illustrated in Figure 1, this DC-DC converter is comprised of two enhanced (eGaN) FET with an input voltage range from 15 – 45 V and a nominal output of 10V. One of the transistors, Q1 is the high side as indicated as GaN1 in the board, while Q2 low sideis indicated asGaN2. They are flip-chip mounted; therefore the surface of them are substrate side. A pair of magnetic field sensors from Ametesis positioned over the eGaNs and connected to DI-1110 data acquisition system by DATAQ. This allows simultaneous measurement of fields of both transistors. In addition, the drain and the source terminals are tapped to measure the terminal voltage and the current between two terminals using an oscilloscope. The measurement set-up for V_{DS} and I_{DS} is shown in Figure 2. The overall experimental set-up is completed using a 3D-printed stand to posit the sensors for our needs.

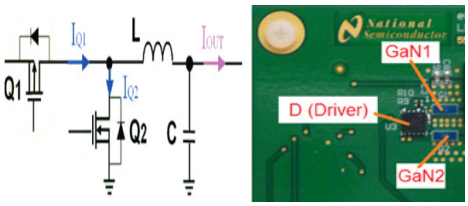

Fig.1. Circuit Diagram (left) and a part of PCB (right) of LM5113 Evaluation Board.

For measurement of normal GaNs, one converter board is maintained at normal operating input voltage of 45V, so that the GaNs on the normal board remains in safe and normal operating conditions (herein referred as pristine GaN).The other board, for overstressed condition, is first overstressed with 50V, allowed to cool to room temperature and then operated at normal 45V at which magnetic field strength is measured. In electrical stressing, load power of the converter has been increased cyclically to see the impact of load current and the channel current in the magnetic field strength change. In terms of the load resistance, it changes from 20 Ω to 1.5 (normal range) to 1.11Ω (stressed condition) controlled by an electronic load system. The loads are changed every 20 minutes to allow cool-down. The choice of the time is based on our preliminary experimental finding that the transistor bulk attains steady surface temperature within 20 minutes. Although, the two transistors, the high-side (Q1) and the low-side one (Q2) are measured simultaneous, the high side transistor is primary focus.

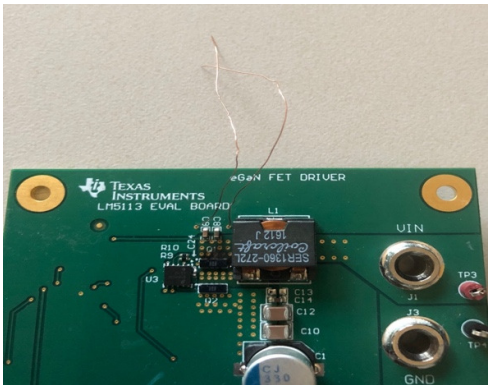

Fig. 2.V_{DS}, I_{DS} measurement configuration. The tapped out cable is connected to a scope.

III. Results and Discussion

A. Drain-Source voltage and current

There has been no significant change in the I_{DS}, which means that, in both pristine and the stressed GaNs, the channel current maintains its respective amount under the same loads. However, there is a visible change in the V_{DS} as I_{DS} changes over different loads as illustrated in Figure 3. This change made some significant change in the ratio of the voltage and the current, the apparent dynamic $R_{DS\text{-}ON}$, shown in Figure 4. It turns out that the apparent $R_{DS\text{-}ON}$ of the stressed GaN manifested average of 57% increase over that of the pristine one. Dynamic $R_{DS\text{-}ON}$ is attributed to traps during electrical stressing, where for on-state, electrons are entangled in traps near the channel [8], which decreases device conductivity. Our experiment shows that the apparent $R_{DS\text{-}ON}$ of stressed GaN is increased when it is returned to normal operating condition after the over voltage (50 V) condition.

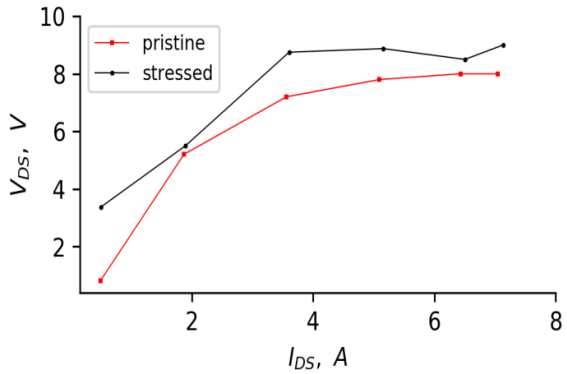

Fig. 3.Drain-Source voltage as function of Drain-source current.

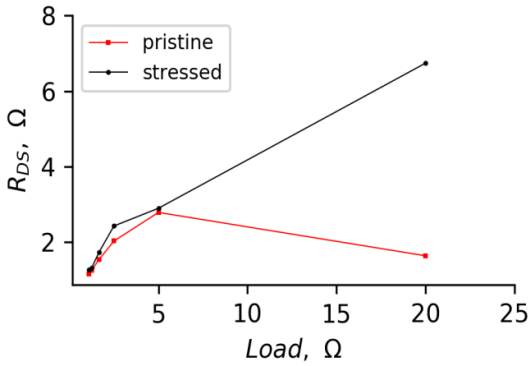

Fig. 4.Dynamic on-state resistance. Note the drastic increment at normal load.

The drastic increment at normal load, 20 Ω, illustrates the persistence of electrons in trapped states and a decreased conductivity in the stressed device. Thus, it is inferred that there is significant change in material microstructure and band offset of AlGaN/GaN interface in the stressed device becausemicrostructure affects bandgap, which in turn moderates semiconductor conductivity and band offset in heterostructures. N-channel of AlGaN/GaN is guaranteed by conduction band offset (CBO) by the following relationship [9]:

$$CBO = E_g(x) - VBO - E_g^{GaN} \quad (1)$$

where$E_g(x)$ is bandgap of $Al_xGa_{1-x}N$ and VBO is the valence band offset. The surface temperature of pristine device at 20 Ω is 30°C and it implies much higher value within the bulk. Such high temperature has been observed in GaN layer of GaN FET [10]. The high bulk temperature may induce gradual or rapid annealing of GaN layer depending on whether device is in normal or stressed condition. Hence, we infer that over voltage enhances annealing over time within normal operating conditions. At stressed condition, there is increased joule heating and the attendant annealing can lead to cracks as well as enhance other prior existing structural defects (dislocations etc.); thereby increasing the density of trap centers at interfaces and bulk of the GaN FET. The fact that $R_{DS\text{-}ON}$ of stressed GaN FETs remains high after stress validates this inference. The 'burn out' of the device witnessed in reliability experiments may be attributed to this increment in joule-heating.

B. Magnetic Field Strength

Next, we conjecture that alteration of material property is reflected in the magnetic field strength under the same channel current of loading. The trap and relaxation (de-trap) in the GaN/Substrate interface is similar to displacement current, such that the magnetic field for fixed$I_{DS} \gg I_T$is expressed as

$$B = \mu I_{DS} + \left[\mu I_T + \mu\varepsilon\frac{d\Phi_E}{d\tau}\right] (2)$$
$$\approx \mu\left[I_{DS} + \varepsilon\frac{d\Phi_E}{d\tau}\right]$$

where, I_T is current due to temperature gradient in the bulk, Φ_E is Seebeck electric flux moderated by charge density at GaN/Substrate interface, τ is relaxation time, and μ and ε are the global permeability and permittivity of the bulk.

We compare the magnetic field strength measured by the magnetic sensor and the drain-source current for pristine and stressed GaN FETs in the same loading condition, the current of which is assumed to be proportional to the channel current. As illustrated in Figure 5, the noticeable increase of magnetic field strength in the stressed GaN in comparable currents shows that material properties of the bulk are changed during the stress. Another notice is the non-linearity of magnetic field strength to the channel current, which infers additional significant contribution from temperature dependent charge transport in the bulk to that from the above mentioned space charge at GaN/Substrate interface.

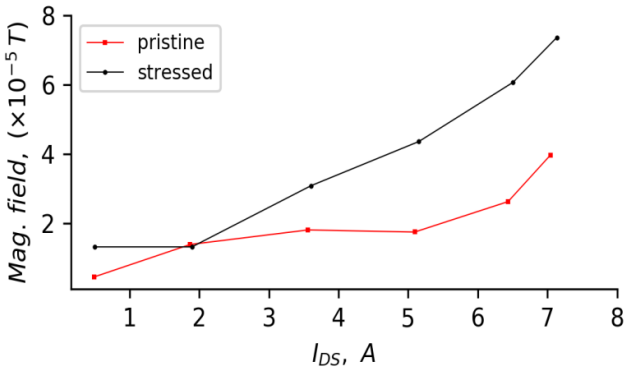

Fig. 5.Magnetic field strength of pristine and stressed GaN FETs.

It is an interesting finding that Eq. (2) may isolate two material parameters of interest as an indicator of health status of circuit-mounted GaN FET. Moreover, it opens the window for in-depth study of ε or μ to correlate with magnetic field strength and material property alteration.

IV. CONCLUSIONS

It has been experimentally demonstrated that degradation of in-operation GaN FET, through the changes in electrical material properties of the bulk, manifested in a surface observable parameter such as magnetic field strength change in comparable channel current. The experimental investigation revealed that permittivity and permeability of the heterostructure were properties of interest under stressed condition, extended study of which, correlated with the magnetic field strength under the same current, would hope to yield a robust model for real time tracking for internal defect detection of circuit-mounted GaN FET devices in operation.

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