Chapter 1. Introduction

Intel 4004, a 4-bit CPU built with 2300 transistors, was the first single chip microprocessor, originally designed for Busicom, a Japanese calculator company, and its right bought back after the company was in trouble. Even though the data was processed in 4 bits, its instructions were 8 bits long. Program and Data memory were separate with a 1K data memory and a 4K program memory, and it was the first Harvard architecture (see the following for computer architecture).

Since Intel 4004, following the Moore's Law, CPU experienced leaps and bounds in the number of bits, the size of memory, and the speed. However, the internal structure of processor has not changed much: the structure shares a common organization. A computer System consists of CPU (with PC(program counter), Registers, SR(Status Register)) and memory. Computer architecture is the way CPU and Memory are organized. Another way to describe the computer architecture is by instructions and their executions.

The two architectures by the CPU and Memory organization are Von Neumann architecture which has one common memory for both instruction and data. This architecture is also called the Princeton architecture. The other architecture is Harvard architecture which has two separate memories: one for instruction and the other for data.

By instructions and the their execution, we have Complex Instruction Set Computers (CISC) architecture and Reduced Instruction Set Computers (RISC) architecture. CISC is characterized by variety of instructions for complex tasks and the instructions of varying length. On the other hand, RISC has fewer and simpler instructions than CISC. The instruction length is the same so that pipelined instruction execution is possible.

CISC is the Computer architecture prior to mid-1980's notably of IBM 390, Motorola 680x0, and Intel 80x86 processors. The basic fetch-execute sequence is designed to support a large number of complex instructions. And this approach brings complex decoding procedures and complex control unit. One instruction achieves a complex task in CISC.

One the other hand, RISC is the Computer architecture after mid-1980's, notably with the following processors and computers: IBM 801, SUN SPARC, MIPS, HP PA-RISC, IBM RS/6000, and PowerPC. RISC architecture comes with a small set of simple instructions and, by adopting pipelined architecture, overlaps many concurrent operations.

The PIC16F877 of Microchip Technology Inc., the main CPU of this book, is a RISC processor with Harvard architecture. The origin of the PIC processor is the Harvard architecture (with two separate memory structure) of the DARPA project, which was defeated in competition by Princeton architecture (with single memory structure). However, the idea of the Harvard architecture was picked up and made in to a series of processors called Signetics 8x300. Later, General Instruments further improved the Signectics processor and introduced the new one as PIC (Peripheral Interface Controller), and, as the name implies, it compensated the poor I/O design. In 1985, General Instrument spun off into Arizona Microchip Technology, which later became the current Microchip Technology Inc.