EECE-404 Senior Design 2

DOPES (Diagnostics of Power Electronic Systems)

FINAL REPORT

Submitted by:

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Summary

Technology and its advancement with respect to hardware rely heavily on the integrity of the power electronic components that are found within them. With that integrity in mind, the DOPES project objective in the long run is to create an embedded real –time sensor network to detect external characteristics of critical components, with an established mathematical formula that defines failure definitively. This formula and sensor network would be used to predict component failure, and provide a reflexive recovery mechanism in the form of altered voltage/current correction in order to pivot the lifetime of the component away from failure and into stable operation. Taking into account design requirements within the limitation of constraints and other methods of spectroscopy, a unique approach was achieved to bring into fruition the DOPES academic year goal for the project.

Problem Statement

In accordance with Ampere’s law and the laws of thermodynamics, the current carrying power electronic components (GaN transistor in the scope of this project) radiates a magnetic field and also increases in heat; both characteristics which can be measured and analyzed. It is through these parameters that DOPES seeks to characterize failure using mass data analysis to extract some mathematical correlation.

The long term goal of the DOPES project is to create a coupled embedded sensor network with established mathematical definitions of failure in a component, along with a recovery system for said component to decrease electrical stress and produce product longevity.

The academic year goal for the DOPES project this year was to create the sensor network and extract data pertinent to determining or characterizing a failure in GaN transistors as a function of temperature and the magnetic field.

Design Requirement

Taking into consideration the academic year goal and that of the overall project goal, the design that was developed had to fit within a framework of specific details.

- Sensor accuracy in data apprehension within 1% of actual value
- Apparatus ability to operate in temperatures from 65-300°C
- Sampling rate (range) for data acquisition 1-100 readings/ms
- Total cost below $300

Constraints

The project's constraints were mostly restricted to time boundaries, in that the construction of the sensory network was just one element or cog in a larger research group. In order to facilitate an overall better workflow to the larger group, a restriction of about 2-3 months to develop and implement the design was enforced.

Sourcing and procurement of one of the designs initialized was scheduled to be manufactured by another university. However, due to fabrication incapabilities at our collaborative university, third party manufacturers of Printed Circuit Boards had to be contacted and selected as the industry partners that would realize the designs generated.

Current Status of Art

Figure 1.0 Showing Impedance Analyzer

In today's market, current extensive research has shown that there are no commercial tools available that function the way the DOPES group's design is intended to function. Failure however, has been known to be characterized as a function of the components impedance. Fig 1.0 shows what is called an **impedance analyzer**. It works by applying a special voltage across the component at question and measuring the current and phase angle through it. Using Ohm's law (V = IZ), the impedance is then calculated. This device however, is not useful to DOPES for the following reasons:

1. Extraction method is intrusive – Our DOPES projects proposes a method of obtaining failure characteristics through the observations of parameters that can be obtained by non-contact methods. To obtain the impedance using the analyzer, physical probing must be done to the component. In our case with the GaN transistor, probing and the supplication of voltage will alter the overall functionality of the buck converter system, which is an outcome that is not desired.
2. Economics – Impedance analyzers are expensive, especially as one tends towards obtaining higher resolution data or an increased frequency range; from around $4000-$6000+. This far exceeds the budget available for this year's academic goal.

Solution Design

The period of development that was available for DOPES was strongly active, with many designs being brought to fruition. However, the common driver from the iteration of each new design was the enhancement of data extraction.

Design 1.0 – scanning arm

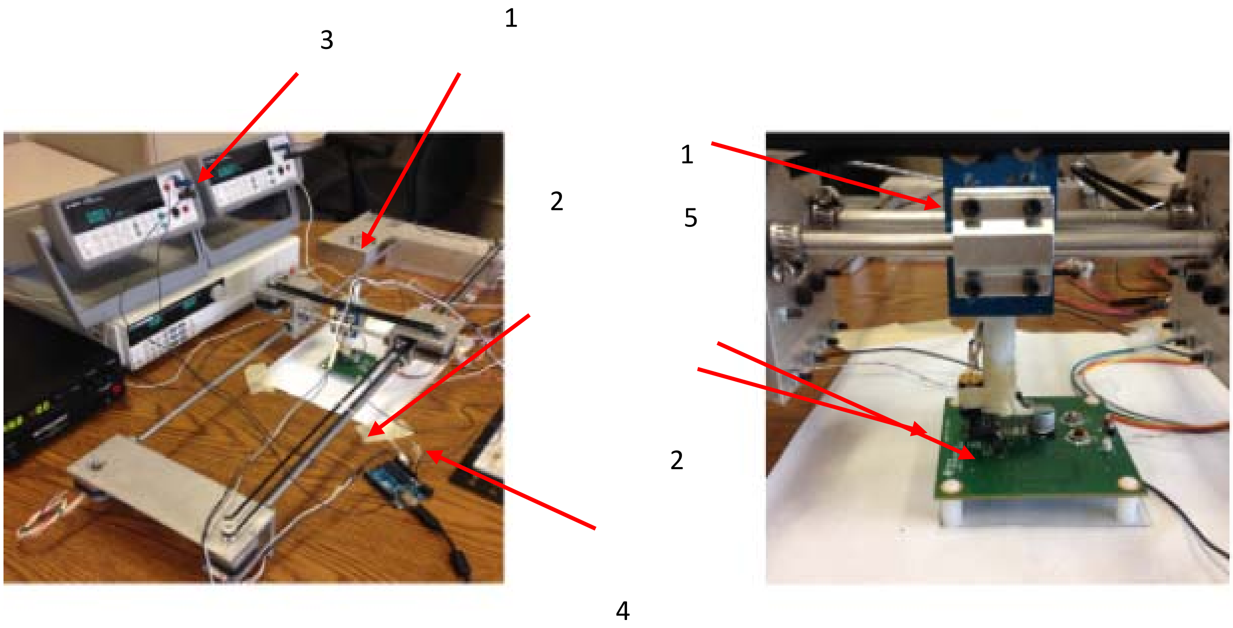


Figure 2.0 showing Design 1.0

This design features a moving arm **1** which oscillates in a strategic predetermined pattern along the LM5113 (buck converter) **2.** Within the moving arm **2** are the sensors of interest **5,** which extracts data via the data acquisition module labelled **4.** The moving arm **2** would operate while the buck converter **2** would be subject to different load conditions as was designed so a set excursion schedule.

From this setup, meaningful data was obtained for the most part. However, it proved to be a challenge making sense of a lot of the data in that data was also collected for non-essential parts of the board. It was determined that a lot of the time spent in filtering out non-essential data. So, in order to move forward and acquire better data, a new design had to be implemented.

Design 1.1a – stationary sensor network

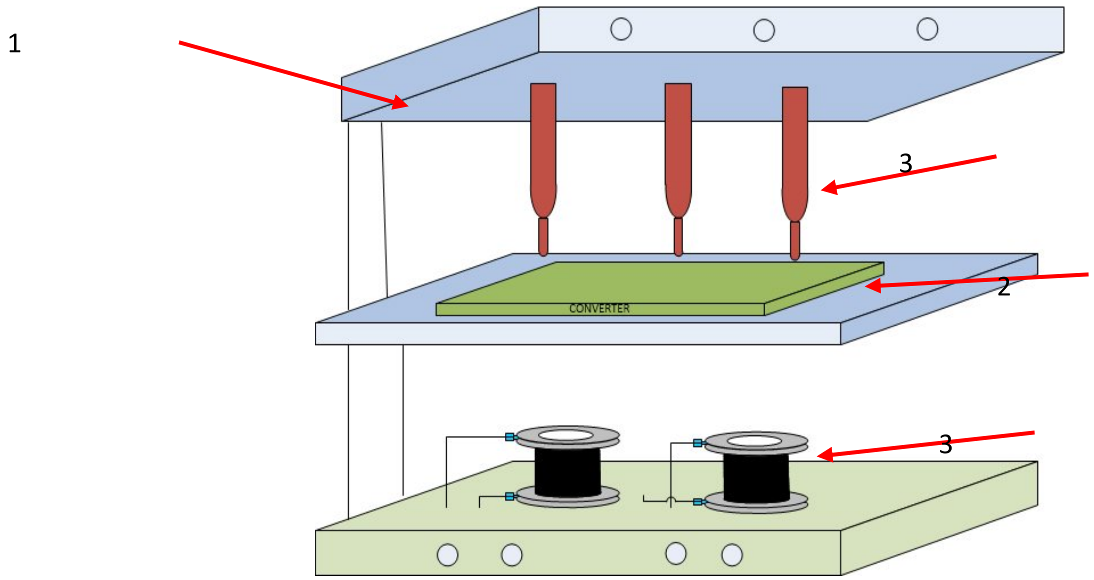


Figure 3.0 showing design 1.1a

This design consisted of a 3D printed table **1** with our buck converter **2** centered and our sensors **3** placed over key components only. The data extraction system **4** was also modified to increase automation.

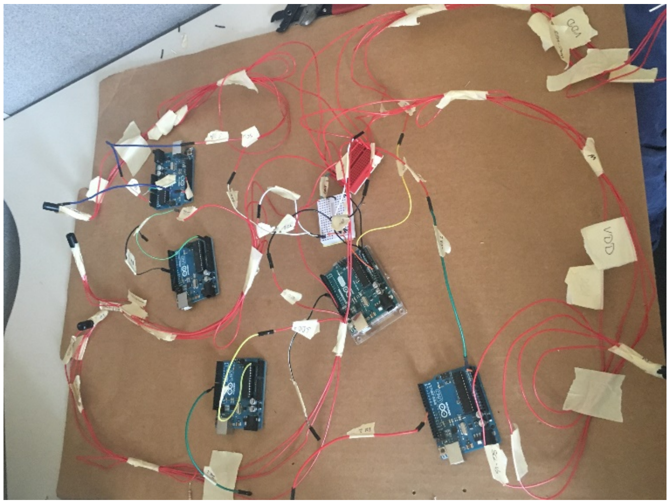


Figure 4.0 showing Sensory Network created for use in Design 1.1a

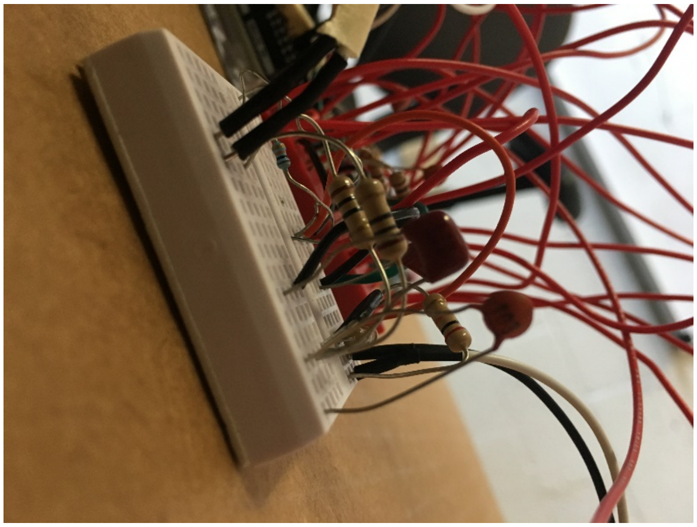


Figure 5.0 showing filters designed and implemented for use in new data extraction

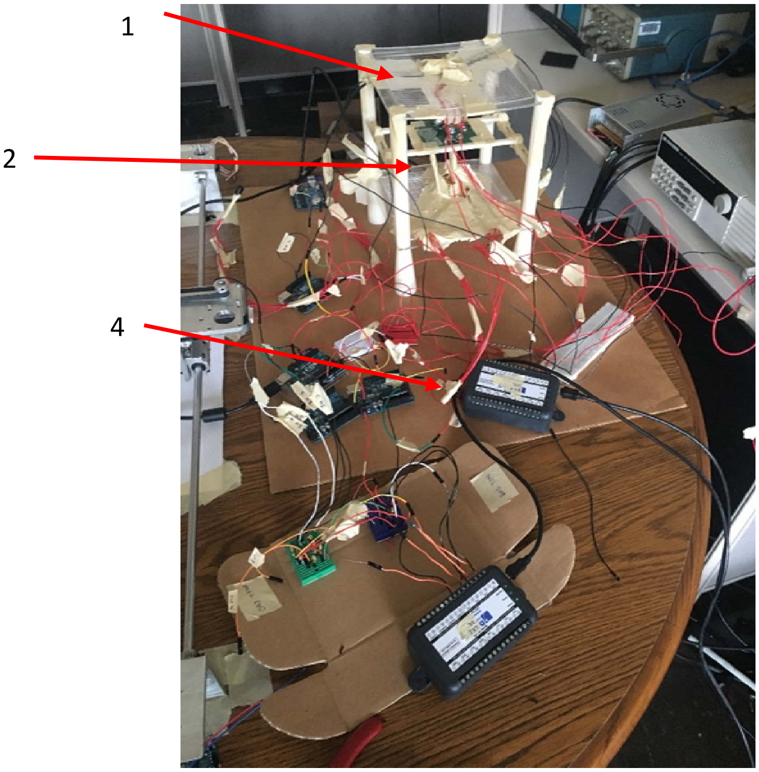


Figure 6.0 showing overall setup of Design 1.1a

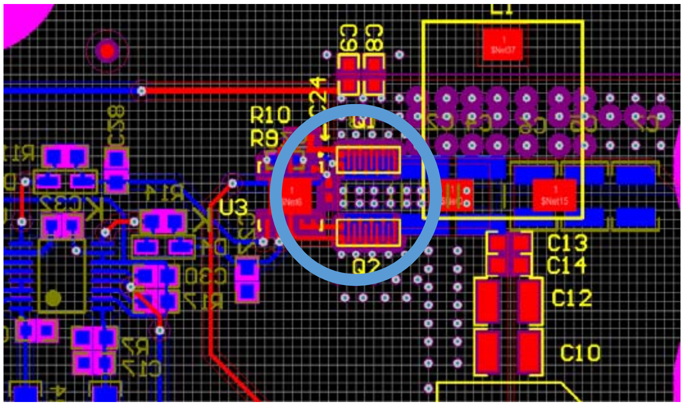
Design 1.1a pros:

1. Automation – this setup allowed us to run excursion patterns for even longer due to the automated data extraction system,
2. Precision – because we no longer scanned non- essential components, the concentration of the accuracy of our data increased.

Design 1.1a cons:

1. Size – In moving towards our embedded sensory network goal, design 2 does not provide a great model to reflect our objective
2. Board swapping – because of how the converter is embedded in the 3d printed structure, it is very difficult to replace it.

Design 1.1b – PCB Adjustment



Figures 7.0 and 7.1 showing design 1.1c

The solution generated involves reformulating the buck converter on PCB design software from the design files available. Our constraint in the team for our embedded sensors to be placed on the board is space; between critical components such as the transistors (which are being examined) and the driver, there is not enough space to put the sensors. The design modification developed involves orienting the transistors differently and adding pads for the sensors, so that the sensory network can be established. Many routes of PCB trace must also be readjusted in order to cope with the design. At the end of it all, the buck converter should lose no functionality with the modifications we make.

This solution design could not be implemented due to the incapability of our university partner to fabricate the complex design, and also the expensive cost of fabricating it at a 3rd party company.

Design 1.1c – Isolated Transistor

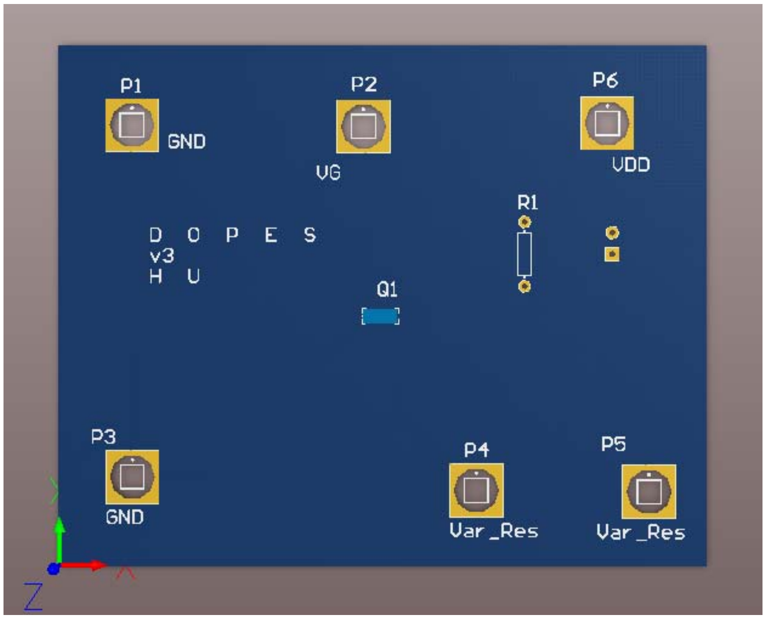


Figure 8.0 showing design 1.1c

Design 1.1c involves the isolation of the GaN transistor and application of the component in a simple switching circuit. This provides the same operation of the transistor in the buck converter circuit (LM5113) with more clearance for the sensors for even more accurate data being acquired. The switching circuit was designed below, with provisions made for altering the load to the system to maintain the excursion schedule.

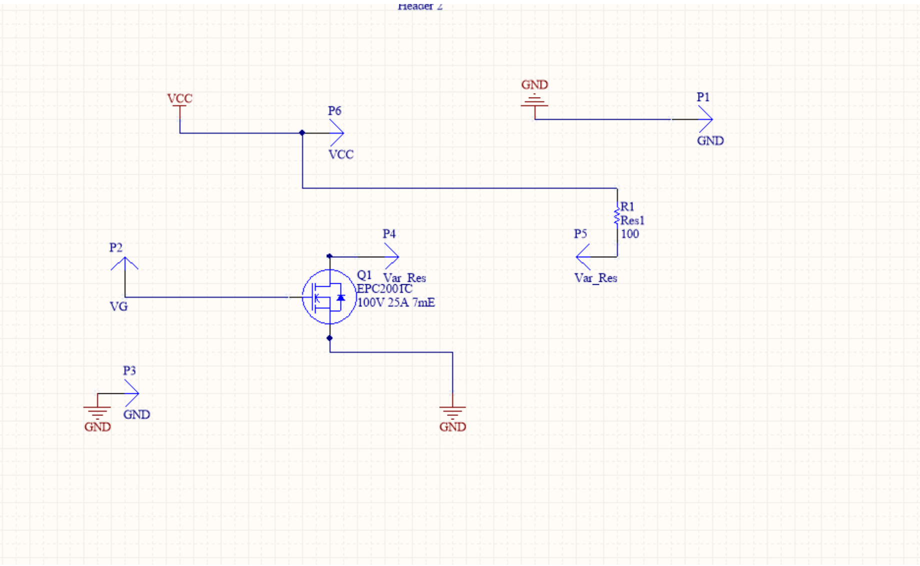


Figure 9.0 showing schematic for design 1.1c

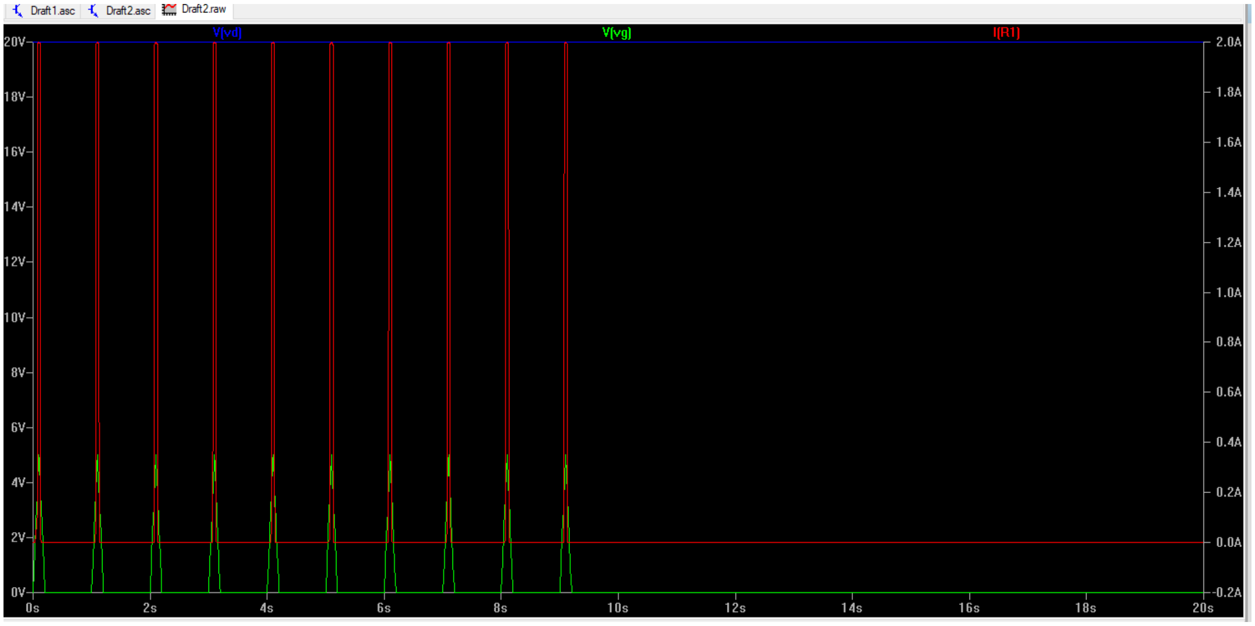


Figure 10.0 showing the simulation verification for design 1.1c

For this academic semester, the focus was the design and implementation of this new design. The circuit was simulated using LTSpice to ensure its integrity, and dispersed to the manufacturer for fabrication.

This design was to be implemented by early April, however the DOPES team is still currently awaiting the delivery of the redesigned PCB from a 3rd party manufacturer overseas.

Project Implementation Plan

Date:	23rd January 2018
Team Name:	POETS
Project Title:	DOPES
Team Members:	Shamar Christian

Month	Week No	Tasks	Member in Charge	Monthly Deliverables
Jan	1			PCB Final Design
	2			
	3	Submission of final	Shamar Christian	
	4	Submission of final design for PCB	Shamar Christian	
Feb	1			Status update on manufacturing process
	2	Feedback from PCB manufacturer	Shamar Christian	
	3	Possible design correction	Shamar Christian	
	4			
Mar	1	Reception of PCB	Shamar Christian	New (physical) system running along side legacy system for data collection
	2	Complete installation of Sensors	Shamar Christian	
	3	Competency test with software	Shamar Christian	
	4	Experimental Procedure	Shamar Christian	
Apr	1	Data Analysis	Shamar Christian	Substantial data for failure characterization
	2	Project Demo + Presentation Event	Shamar Christian	
	3			
	4			

Conclusion

The movement forward dictates the further implementation of Design 1.1c pending the arrival of the new PCB. With this, further refinement of the mathematical model of failure in GaN transistors can take place through obtaining more data. This has significant implications for further research, in that the data can indicate the phenomena physically that is taking place at the atomic level within the GaN. Also, with more data being obtained, the commencement of diagnosis methodologies for failing power electronic components can initiate.

References

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H. Wang *et al*., "Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97-114, March 2014

Physics-of-failure-based prognostics for electronic products

Michael PechtJie Gu *Transactions of the Institute of Measurement and Control*, Vol 31, Issue 3-4, pp. 309 -322 June 2009