EECE404 Senior Design II Electrical and Computer Engineering Howard University
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Webpage: www.mwftr.com/SD1415.html

INTRUDER

PROGRESS PRESENTATION III

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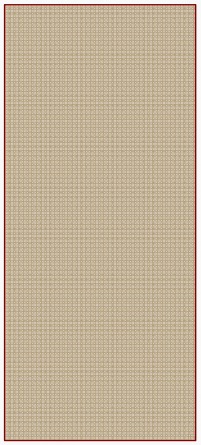


DESIGN REQUIREMENTS

- Intel Chip must authenticate user on computer
  - Must be software compatible with Linux OS
- FPGA must wait for authentication from Intel chip before executing command
  - Similar to “wait for” statement in code
- FPGA must receive command from infrared receiver

MILESTONES

	Date	Milestone	Outcome
1	Feb. 13	Develop scenario/user case	In the Process
2	Mar. 4	Complete patient database	Complete
3	Mar. 6	Complete cryptosystem [connected IR and algorithm]	In the Process
4	Mar. 11	PCI communication	In the Process
5	Mar. 12	Order Infusion Pump or Alternative	In the Process
6	Mar. 31	Complete Assembly & Test	

HIGHLIGHTS

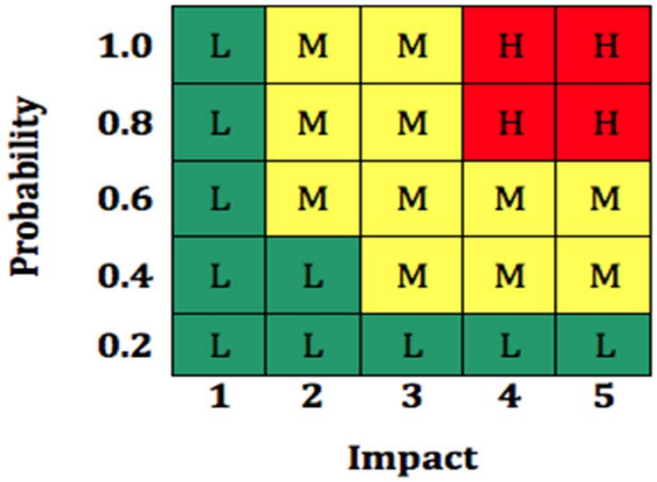
- 3 Functioning components
  - IR Receiver & Transmitter
  - Cryptographic Algorithm
  - Complete database & Interface
    - High-level code (Java)
- Increase in learning and comfort with Verilog, VHDL and Quartus

LOW POINTS

- ModelSIM complications
- Debugging
- Misunderstanding 7-segment display
  - Displays from LSB to MSB (left to right)

RISK MITIGATION

Risk	Probability	Impact	Risk Control & Management
Infusion pump does not communicate or is not compatible with hardware	0.4	5	• Order infusion pump on time • Test with board to confirm compatibility
PCI fails to communicate Intel and FPGA chips	0.6	4	• Attempt new method of approach



DEMONSTRATIONS

FOCUS FOR NEXT PERIOD

- Component connection
  - PCI communication
- Order infusion pump or alternative
- Develop use case

QUESTIONS