SENIOR DESIGN ORAL PRESENTATION

POWER INTEGRITY in Modern Electronics

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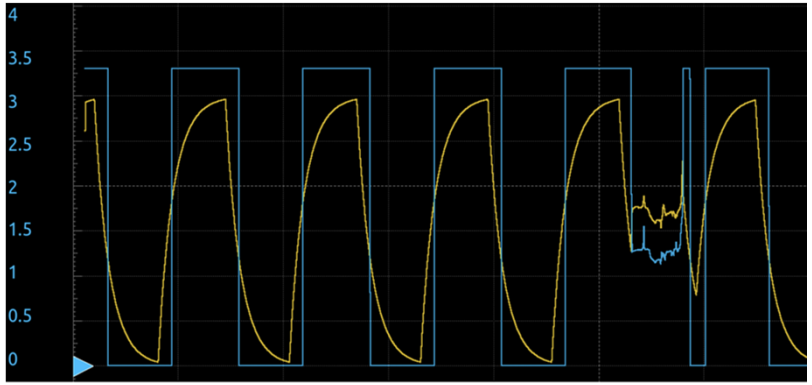
Why(Background)?

- Failure from high speed electronics leading to fluctuations in voltage in power PDN i.e. increases or decreases of the expected voltage
- Failures can be in the form of a malfunctioning system or suboptimal circuit performance.
- PDN noise can be in the form of switching noise, external electromagnetic interference and unwanted modes.
- We want to ensure power supplied is stable and free from significant fluctuations.
- Ensures device performs optimally.



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Problem statement

- Mitigating Power Delivery Network (PDN) noise is essential for efficient power distribution and to ensure proper functioning of electrical systems present in modern electronic devices.
- Our approach is to design a power delivery network for a common circuit found in modern electronic devices and evaluate power integrity for that circuit, then simulate, fabricate, and test PCBs for it.
- Our design ensures proper identification and evaluation of different noises in the power delivery network of the specific circuit thereby resulting in optimal power integrity for the system.
- It's a better evaluated study of the specific circuit with a precise validation system for debugging that will be beneficial to other engineers while incorporating that specific circuit to other complex systems.

Design requirement - Product specifications

Inputs: 3.3 V - 9 V
Outputs: 8 mA - 32 mA Oscillating Signal
Dimensions: 3 - 9 $inch^2$
Operating limit: 10MHz - 10GHz
Weight: 0.4 lbs - 0.6 lbs
Platform/Hardware: 1) Custom PCB for a Ring Oscillator
2) Custom PCB as a Motherboard for an FPGA

Design requirement - Constraints

Environmental Constraints

- PCB will be made partially of copper as it can be reused even when the device has stopped operating.
- PCBs are free from hazardous materials, making them safer for consumers and reducing environmental contamination (RoHS)

Socio-cultural Constraints

- Documentation for users to be available in various languages to account for different cultures and backgrounds
- PCBs will be color-coded by considering the market requirements and user needs. For eg : Apple prefers black colored PCBs.

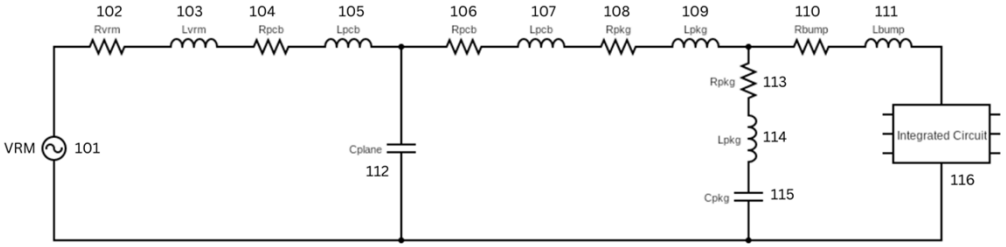
Design requirement - Constraints

Compliance (Rules, Regulations, and Standards)

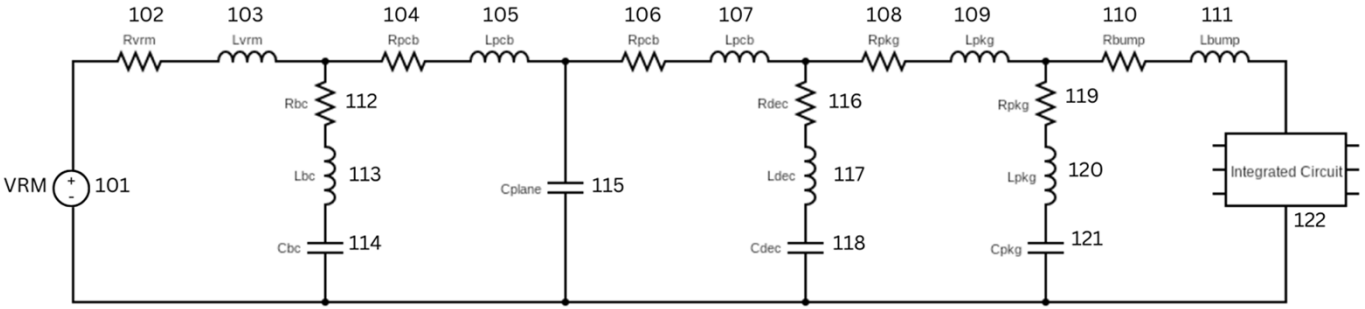
- Electromagnetic Compatibility Compliance (EMC)
- Electronics Standard set by IEEE
- Underwriters Laboratories Certification
- RoHS Compliance (Restriction of Hazardous Substances Directive)

Possible Solutions Design

Solution 1: Power Delivery Network with only IC load



Solution 2: Power Delivery Network with Decoupling Capacitors:



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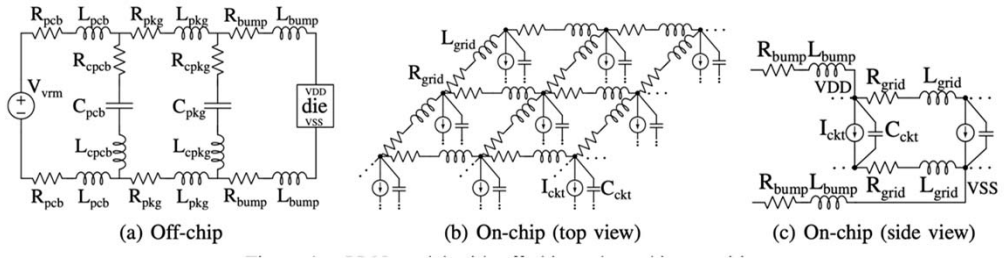
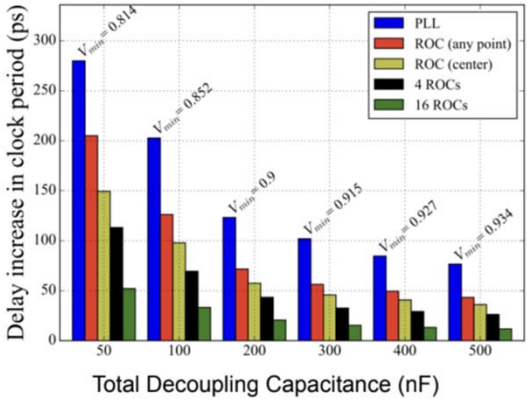
Possible Solutions Designs

Solution 3: Power Delivery Network with Ring Oscillators





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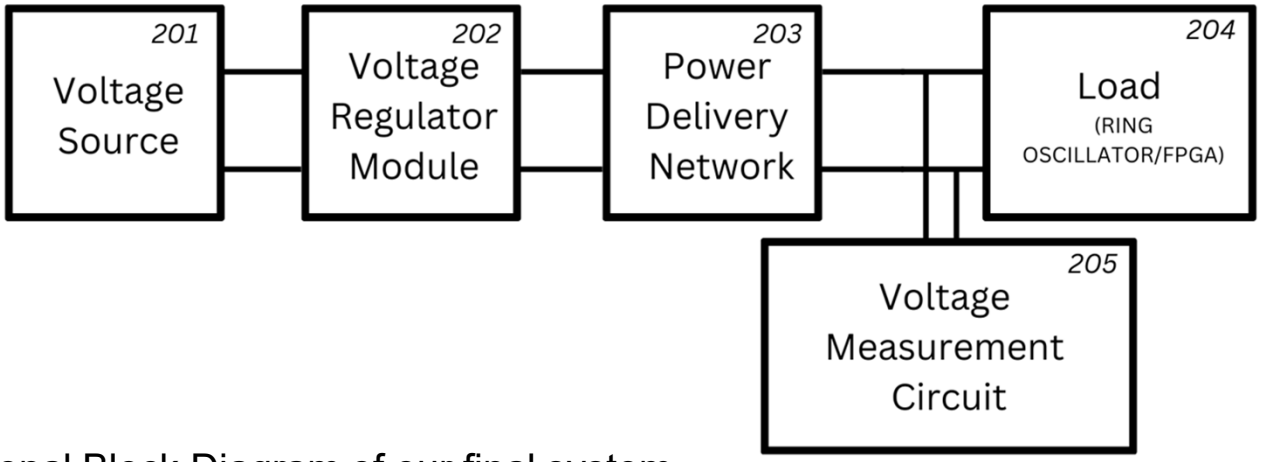
Selection of Top Design

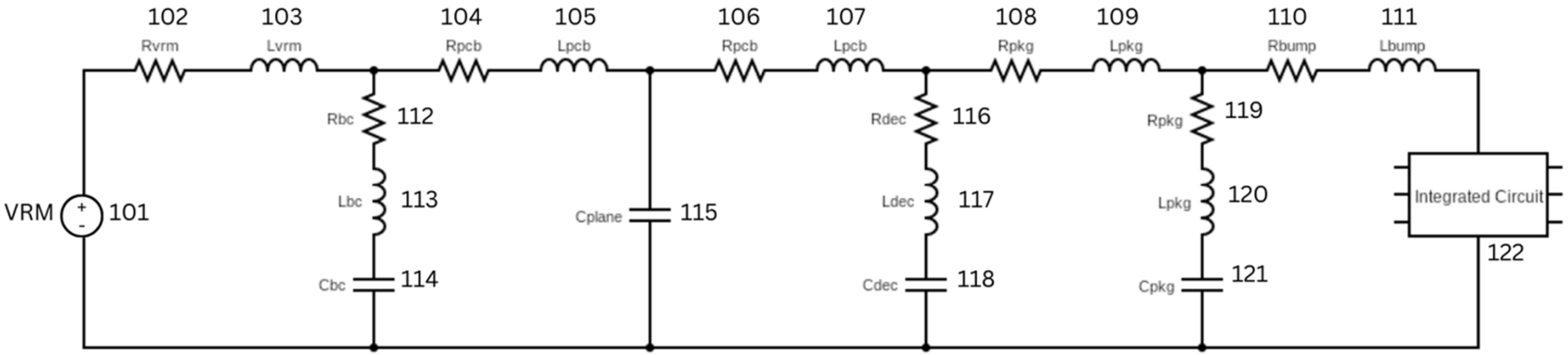
	Wt	Design 1	Score	Agg Score	Design 2	Score	Agg Score	Design 3	Score	Agg Score
Size/weight	1	A simple PCB with a Power Source, a voltage regulator, and an IC.	5	5	A PCB with a power source, a voltage regulator, decoupling, and bulk capacitors	4	4	A PCB with a Power Source, a Voltage Regulator, fewer decoupling and bulk capacitors, and additional Ring Oscillators	3	3
Noise Mitigation	4	Highly susceptible to noise.	1	4	Better PDN Noise Mitigation	4	16	Best design for PDN noise mitigation	5	20
LF /HF Functionality	3	Works properly with LF devices	1	3	Works well with HF as well as LF models.	5	15	Works the best with all the HF and LF designs	5	15
Power Consumption	2	Fewer components to be powered	5	10	The additional capacitors consume more power.	3	6	More components that consume power	4	8
Ease of implementation	5	Can be designed easily	5	25	Easy to design	4	20	Harder to implement because of the addition of the Ring Oscillators	1	5
Total	15			47/65			61/65			51/65

Top Design Solution - Block Diagram



- The Functional Block Diagram of our final system.
  - Voltage Source - DC Power Source
  - VRM - Maintain a stepped down constant voltage output
  - PDN - Two port Transmission Line
  - Load - Ring Oscillator that draws fluctuating voltage
  - Voltage Measurement Circuit - Oscilloscope/Voltage Network Analyzer
- A ring oscillator is a device composed of an odd number of NOT gates in a ring, whose output oscillates between two voltage levels, representing true and false.

First Order Power/Ground Plane Model



- Two port network considering parasitics and lumped RLC models for all parts of the final design.

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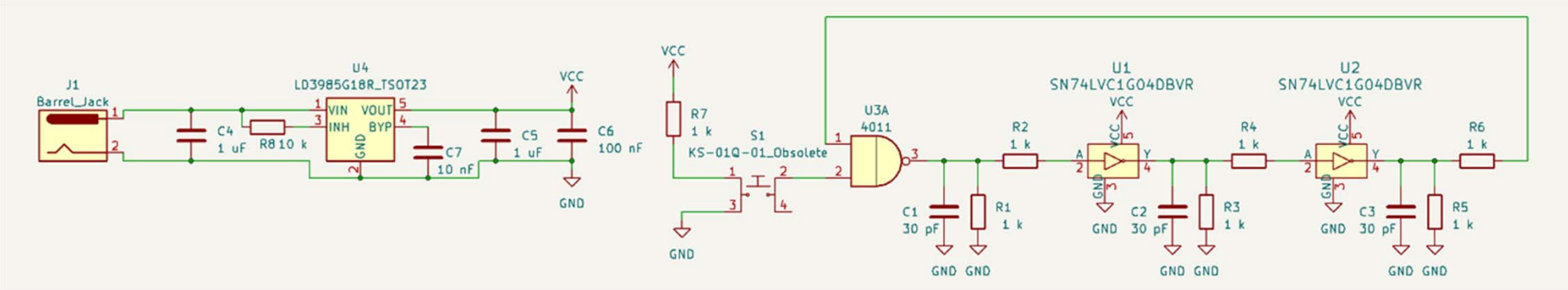
Component Model



J1 - Barrel Jack Connection to Battery Pack Module

U1, U2 - Inverters for Ring Oscillator

S1 - Reset Button for the Ring Oscillator

C4 - Input Capacitor to the VRM

C6 - Decoupling Capacitor

Bypass Capacitor for the VRM

U4 - Voltage Regulator

U3A - NAND gate - Trigger for Ring Oscillator

C1, C2, C3 - Load Capacitors

C5 - Bulk Capacitor

C7 -

Component Level Selection - Load

1) Inverter / NOT gate x2	
THT 6 Circuit Package	**SMD 1 Circuit Package**
• Excess NOT gates on the same package that can add unused components or unnecessarily consume power • More vulnerable to cross-talk and interference as there are multiple circuits within the same package • Difficult in testing the circuit as limited access to intermediate paths • THT, generally, has more parasitic inductance and capacitance than SMD	• Can precisely choose the right amount of inverters needed with no unused components in the circuit • One circuit in one package spaces out the different NOT gates • More accessible testing as each part is separated and the circuit could be organized for testing as required • SMD, being closer to the PCB surface, have lower parasitic inductance and capacitance compared to THT
FInal Selection: SMD 1 Circuit Package	

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Component Level Selection - Load

1) NAND gate x1	
THT 8 Input Package	**SMD 2 Input Package**
• Gate with excess number of inputs, all alternatives in THT packaging had extra inputs • THT, generally, has more parasitic inductance and capacitance than SMD	• Right number of input gates • SMD, being closer to the PCB surface, have lower parasitic inductance and capacitance compared to THT
Final Selection: SMD 2 Input Package	
2) Capacitors	
Thorugh Hole Technology	**Surface Mount Device**
• THT, generally, has more parasitic inductance and capacitance than SMD	• SMD, being closer to the PCB surface, have lower parasitic inductance and capacitance compared to THT
Final Selection: SMD Device	
3) Resistors	
Final Selection: THT Resistors due to availability and ease of assembly	

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Component Level Selection - Voltage

Voltage Source 201		
Requirements	**Components and Alternatives**	**Description and comparison**
1)Power Source: Output: 5V	**a) Battery Source**	• **4 AA batteries, each labeled to be 1.5V.**
	b) USB	• **USB connected to power source eg: laptops.**
Final selection:	**a) Battery Source**	**Portable Power Source and closer to real life constraints**
2)Battery holder	**Battery Holder in case of a)**	**A battery holder for stable power connection.**

Component Level Selection - Voltage

Voltage Regulator Module (VRM) 202				
Requirements	**Components and alternatives**	**Description and Comparison**	**Purchasing**	**QTY**
1)VRM: Input = 5V Output = 1.8V	a) THT	• Through Hole VRM part which is easier to solder to the PCB, to regulate the voltage supplied to the PCB.	THT VRM	1
	b) SMD	• Surface mount VRM part which reduces the inductance in the power distribution network.	SMD VRM	1
Final Selection:	b) SMD	Reduces the impedance in the PDN essential to reduce the noise.	SMD VRM	1
2) Bulk Capacitors: C= 1uF	SMD in case of b)	• Recommended with use of SMD in the datasheet, also used as a bulk capacitor.	VRM Capacitor	2

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Component Level Selection - PDN

Power Delivery Network (PDN) 203				
Requirements	**Components and Alternatives**	**Description and Comparison**	**Purchasing Link**	**QTY**
1)Decoupling Capacitors: A range of values for C.	SMD	• SMD capacitors reduce inductance path acting as a better decoupling capacitor.	0.1 uF 3300 pF 2 pF	3
	THT	• THT capacitors with variable values to test the effects on the PDN	0.1 uF 3300 pF 2pF	3
Final Selection:	SMD	SMDs are smaller in size and are better to use as decap.	0.1 uF 3300 pF 2 pF	3

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Component Level Selection - PDN

2) Oscilloscope Range: 1MHz-100MHz	Model 1	• An oscilloscope available at the school lab.		1
	Model 2	• A portable oscilloscope with 50Mhz range and a built in Multimeter.	Multimeter+Oscilloscope	1
Final Selection:	Model 1	Easily accessible to us at the CEA EE/CPE labs and more economical.		1

Component Level Selection - PDN

3) Vector Network Analyzer(VNA)	Model 1	• A device used to measure and view the S-parameters in the two port network. • Is more economical.	10Khz-1.5GHZ	1
	Model 2	• A device which can be used as both signal generator and VNA with the range of 100KHz to 5.3 GHz.	VNA+Signal Generator	1
Final Selection:	Model 1	It provides essential functions and is economical.	10Khz-1.5GHZ	1

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Component Level Selection - PDN

4) Multimeter	**Model 1**	• **Easily accessible to us at the CEA EE/CPE labs** • **Is to be used to measure V and I throughout the PDN, to calculate Power Noise.**		**1**
	Model 2	• **Portable multimeter, easy to read.**	**Portable Multimeter**	**1**
Final Selection:	**Model 1**	**Economical and easily accessible, we also have required device usage training .**		**1**

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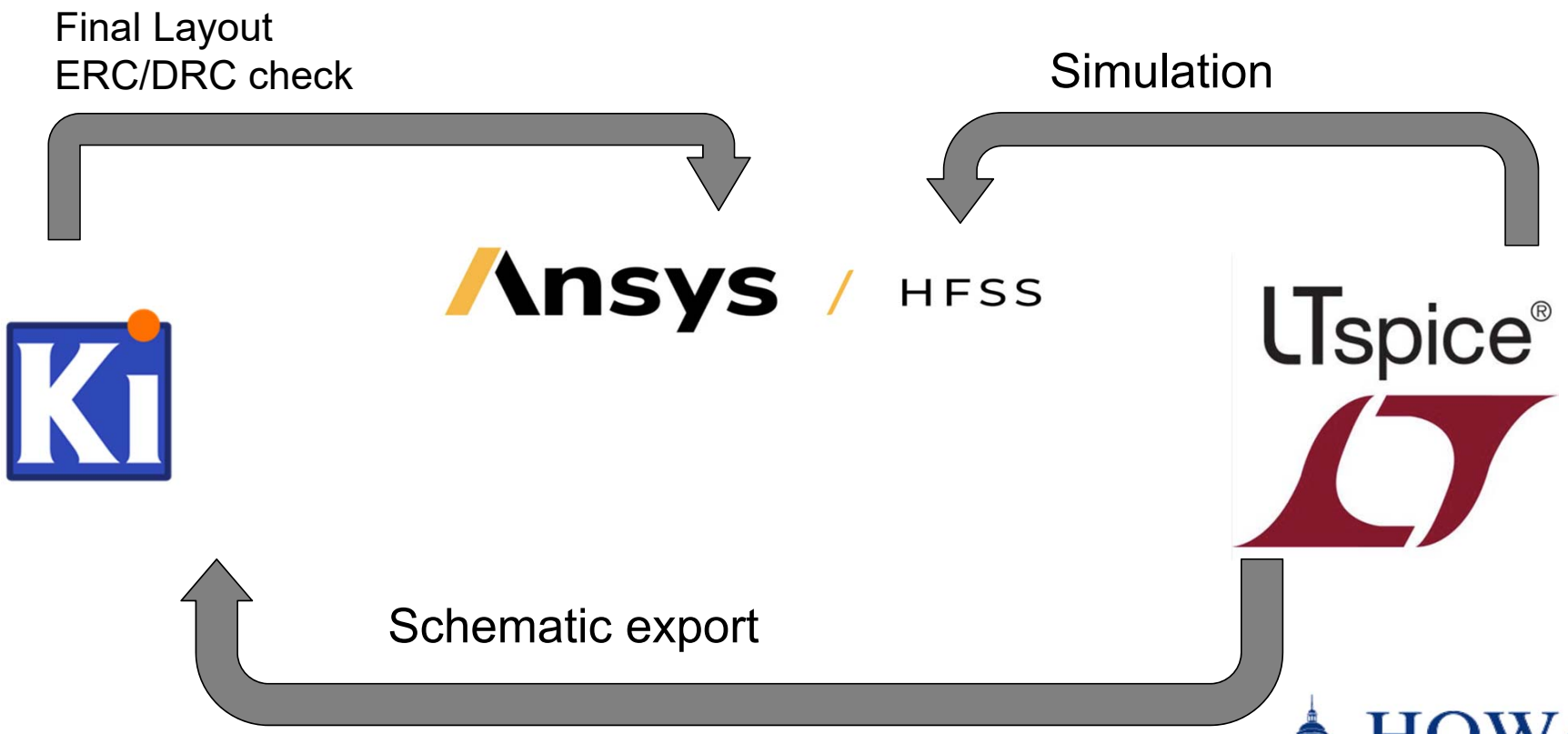
Development Lifeccyle:



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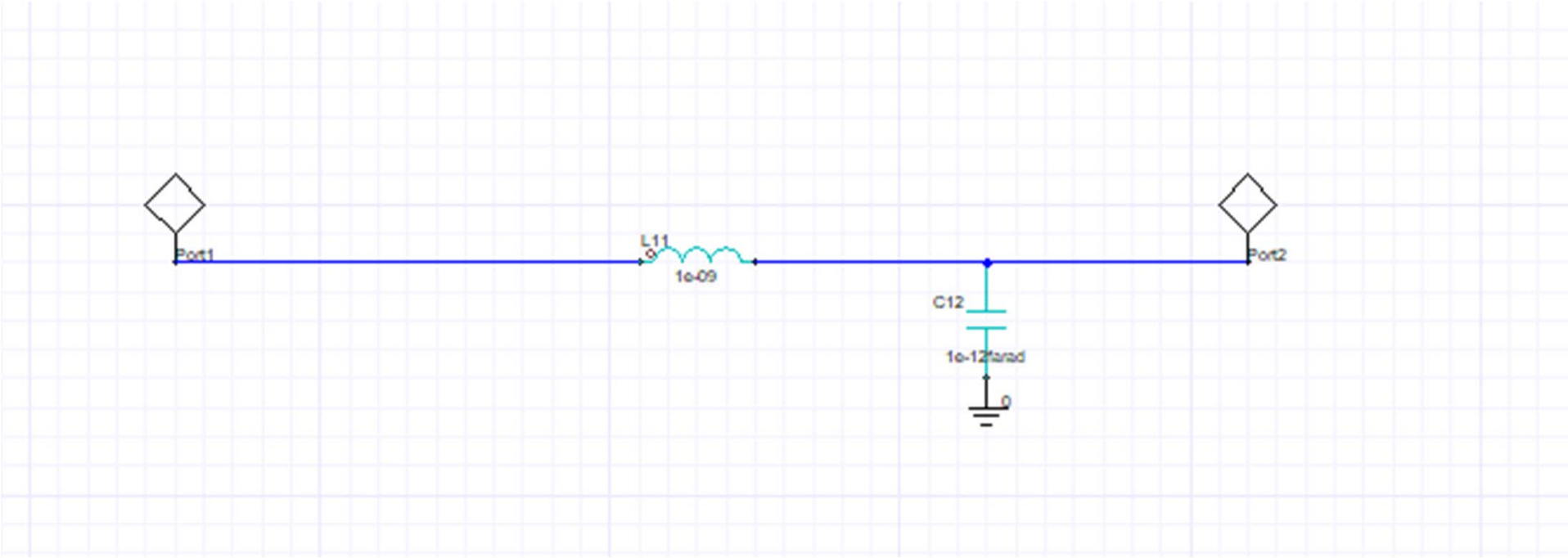
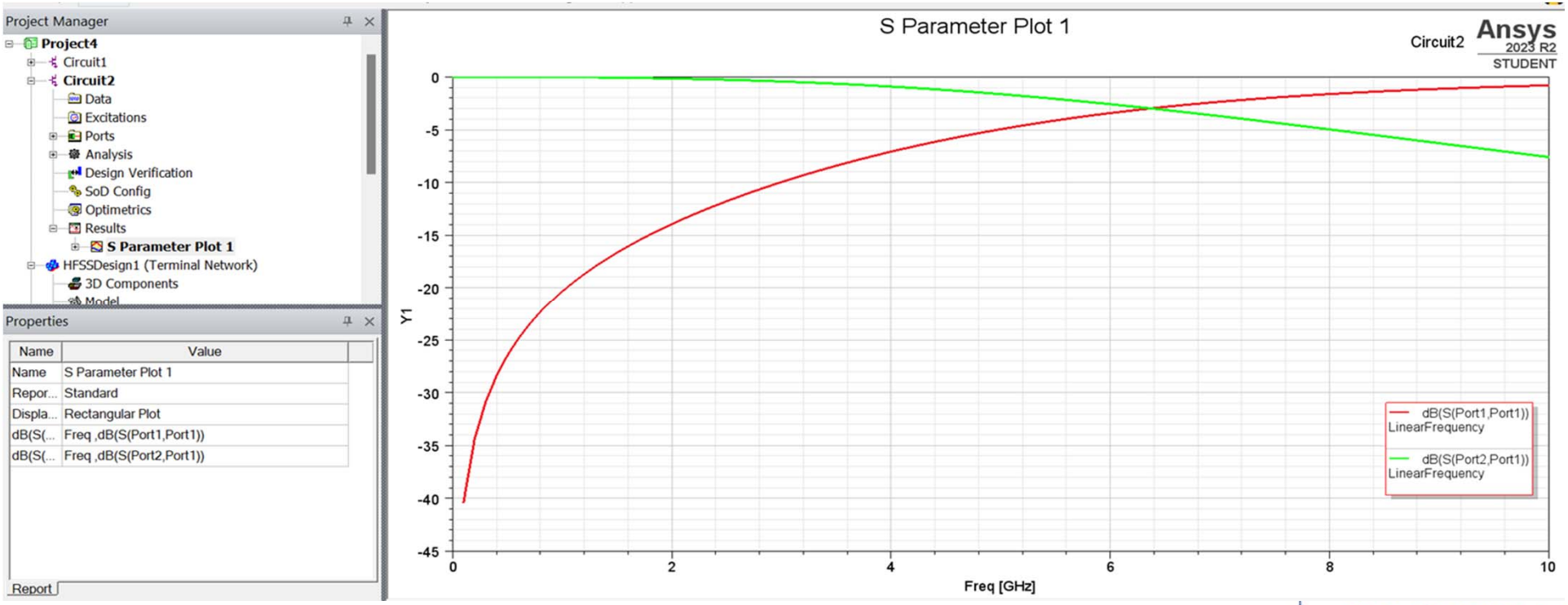
Upskilling Efforts in ANSYS



Upskilling Efforts in ANSYS(Admittance vs f)



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Future/ Next Steps

- Build out complete circuit digital in LTSPICE and do PCB layout in KICAD.
- Do simulations to monitor how voltage and power fluctuates across different components in LTSPICE.
- Use KICAD to build an optimized PCB layout.
- Can import netlist from LTSPICE into KICAD then import PCB design into ANSYS to discover Electromagnetic radiation and interference.
- Receive feedback and reimplement for the second candidate circuit

Conclusion

- **Voltage Fluctuation can render circuits to not function properly**
- **Address this issue with mitigation statistics**
- **Two Candidate Circuits to Emulate:**
  - Ring Oscillator to emulate the IC switching implications
  - FPGA as a backup platform programmed to perform a simple ALU/Memory Function
- **PDN Modelling through circuit and electromagnetic simulation**
- **Designing candidate circuits to showcase the IC switching and thereby the di/dt noise phenomenon on PDN**
- **Create the PCB layout with additional junctions and pads for experimentation and testing**
- **Top Design Solution: 6V DC Input to 140 MHz - 0.5 GHz oscillating signal**
- **Final product could be integrated to other complex systems**

THANK YOU!!!

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