Department of Electrical and Computer Engineering

Howard University

Washington DC 20059

EECE 404 Senior Design II

Spring 2024

Senior Design Final Project

By:

Juwon Wharwood

Victor Iyke-Osuji

Sabien Sykes

Goodness Atanda

Instructor: Charles Kim

Date Assigned: 4/02/2024 Date Submitted: 4/23/2024

Abstract

Our project aimed to develop a functional phase change memcapacitor equipped with a heating element to induce phase transition. This memcapacitor would possess both memory and computing capabilities. We focused on exploring its computing potential, particularly its ability to mimic a varactor or varicap by adjusting capacitance based on the crystallinity of the phase change material.

Initially, we embarked on designing the device's structure and simulating its physics using COMSOL. Subsequently, we planned to fabricate the device into an array of units on a silicon wafer at a fabrication lab in Maryland. Finally, we intended to evaluate the device's performance within a tuning circuit.

We successfully completed the first phase of our project, successfully simulating the device and the heat transfer within the memcapacitor, including the phase change induced by the heater described in our third sprint. Throughout this phase, we iterated on our design several times before settling on the horizontal stack design outlined in our second sprint.

Problem Statement

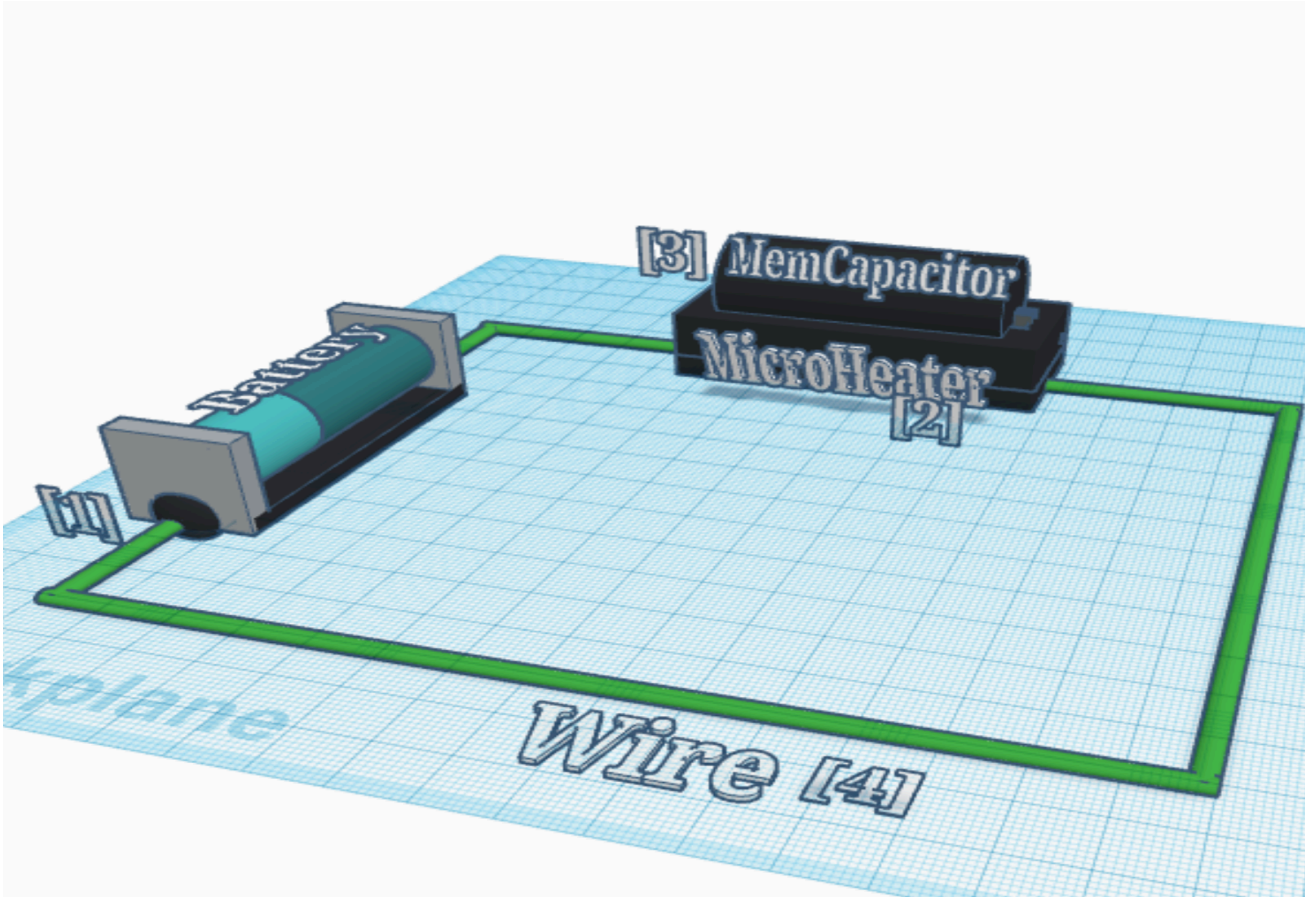
Our project aims to develop a compact phase change memcapacitor with a focus on minimizing power consumption, circuit delay, and cost. This device will preserve the advantages of conventional phase change systems, including non-volatility and rapid switching speeds. The significance lies in providing memory retention without constant power supply, offering greater energy efficiency compared to volatile electrical components. Leveraging the substantial changes in electrical and optical properties of GST, our endeavor seeks to address the demand for efficient and reliable memory solutions.

The overarching objective of this project is to create an innovative variable Capacitor utilizing Phase Change Materials (PCM), with a focus on enhancing speed and non-volatility. Our specific targets encompass the DC, AC, and RF regimes. We aim to demonstrate distinct functionalities enabled by this memory capacitor, showcasing its versatility. Moreover, our goal is to attain a high dynamic range in both capacitance and resistance, ensuring optimal performance across various operational parameters.

Design Requirements

1. Product Specifications:
    a. Phase Change Material
    b. Heater
    c. Small Voltage Source
    d. Small packaging with medium/high heat capacity
    e. High speed circuit
2. Constraints:
    a. Environmental Constraints:
        i. Cannot be used in environments with unstable temperature which could affect the circuit working conditions
        ii. Emissions caused during heating or radical temperature changes
    b. Social-Cultural Constraints:
        i. New implementation for data collection could raise some privacy and security concerns
    c. Compliance:
        i. Data Privacy Standards, thermal safety management, EMC standards outlined by FCC, Electronic device standards outlined by IEEE

Solution Design



The phase change capacitor circuit includes a voltage source[1], microheater[2], memcapacitor[3], and a wire[4] to connect the voltage source to the combined memcapacitor and microheater. In reality, the memcapacitor and microheater are in the nanometer scale, thus, the device would need to be connected to a probe station to provide the voltage source.

The microheater[2] assists the memcapacitor[3] in its phase change process from amorphous to crystalline and vice versa. With an increase in temperature the memcapacitor[3] transitions to its crystalline phase, which is its most effective state at storing and distributing charge. However, at higher temperatures, the material then reverts back to its amorphous state making its ability to release and store charge substantially weaker. Furthermore, this also increases the RC time constant of the discharge of the memcapacitor[3], which decreases the speed of the circuit.

The microheater[2] depends on its own power supply and is designed to work with the phase change material of the memcapacitor[3] in order to have precise increases in heat with small changes in voltage to ensure great control over our system temperature and functionality. The entire circuit is covered with heat resistant packaging to prevent the irregularities in performance due to parasitic effects. The packaging keeps our circuit at regular temperatures ensuring that no performance is lost due to electron-phonon scattering. This is vital because having complete control over the RC time constant is the objective of the design. As a result, other outside influences such as noise and scattering must be mitigated.

Agile Workflow and Weekly Plan

Team Name		Photon 2	
Final Solution Product			
Starting Date of Week (M)	**Sprint #**	**Increment (or intermediate working component)**	**Weekly development tasks**
1/30/2024	1	Produce memristor/heator	k-layout design and multiphysics used to finish design
2/5/2024			Heater will be designed to match multiphysics data
2/12/2024			Fabrications of both devices
2/19/2024	2	Device performance metrics delivered. Memristor and heater are combined to make one device	Design for testing(Functionality)Does device work?
2/26/2024			Design for testing(Performance)Does device match desired specs
3/4/2024			Packaging process begins
3/11/2024			Packaging process ends
3/18/2024	3	Physical system(tuning circuit)	Circuit designed to test device
3/25/2024			Memristor and heater integrated into circuit
4/1/2024			Circuit tested in comparison to industry standard device

Project Implementation Process

Sprint 1

Goals

1. K-Layout design of the devices completed and set up into multiple arrays.
2. Initial COMSOL design of devices have been created based on devices fabricated previously

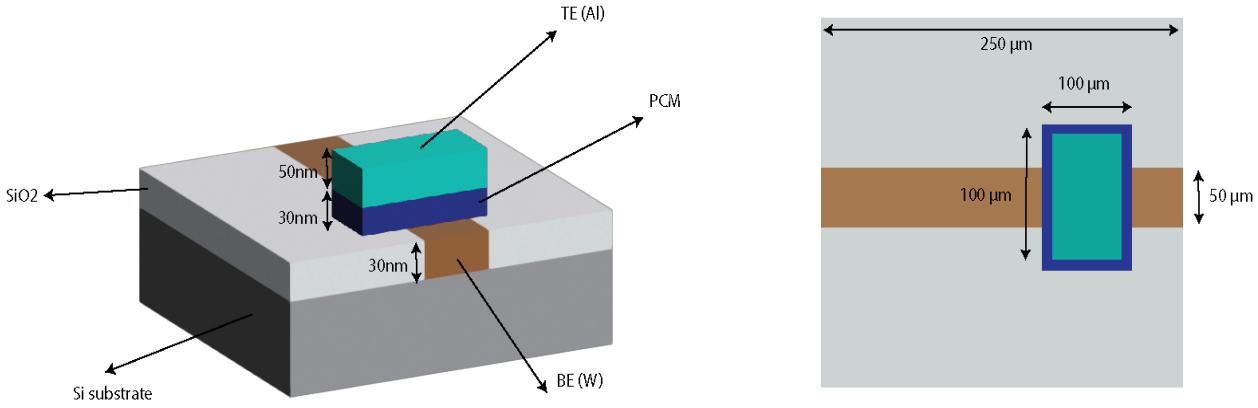
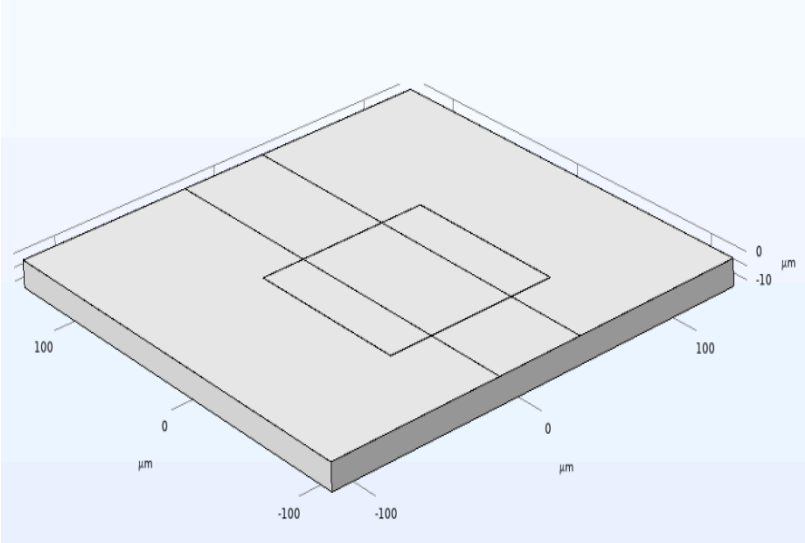
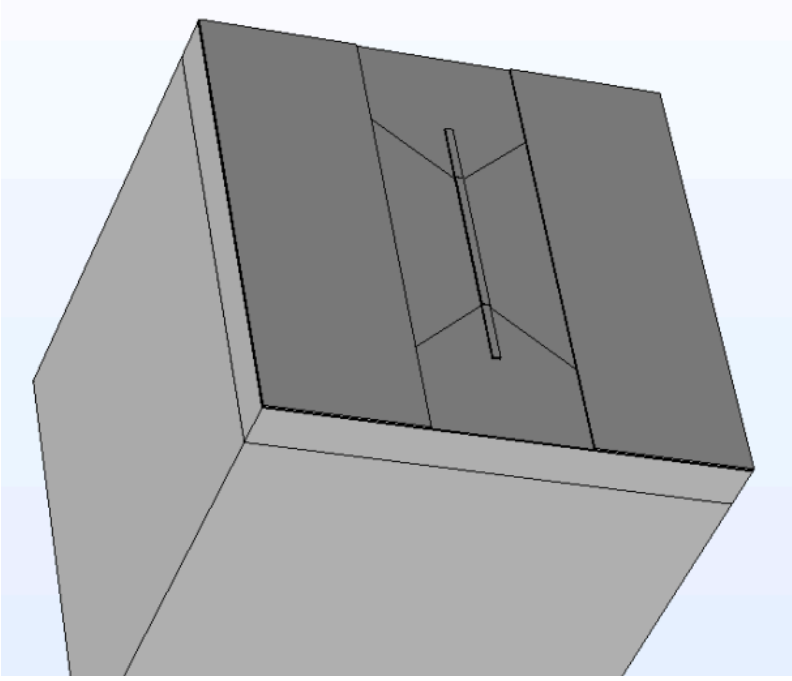


Fig. 1a.
This figure shows the initial design that inspired our Phase Change Capacitor

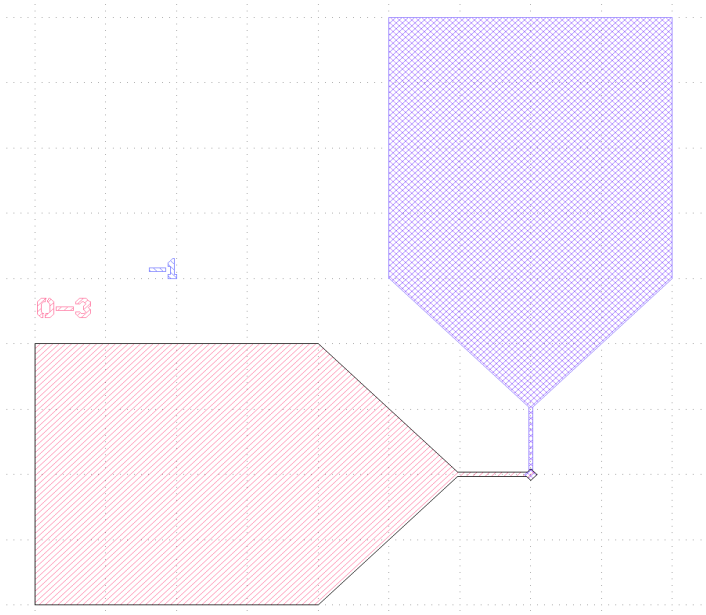
Initial Design of Memcapacitor



Initial Design of Microheater



K-Layout Design of Devices



Sprint 1 Lowlights

1. Device measurements are off by an order of magnitude causing issues with the initial size causing the device to be too large
2. There is not way to connect the two devices in comsol to undergo testing

Sprint 1 Summary

1. Great progress in COMSOL, both structures have been designed and are ready for testing.
2. Initial issues with memristor measurements causing device to be too big
3. Resolution:
4. Based on literature the theoretical device measurements could be calculated including the size of the ITO layer.
5. Devices must be rescaled to match the theoretical size of for heat transfer.

Sprint 2

Goals

1. Determine the desired specifications for indium tin oxide (ITO) layer while comparing layer thickness and surface area with thermal conductivity so that we can see the phase change occur on the vertical stack memcapacitor
2. Deliver device performance metrics and begin experiments to combine memristor and heater to make one device

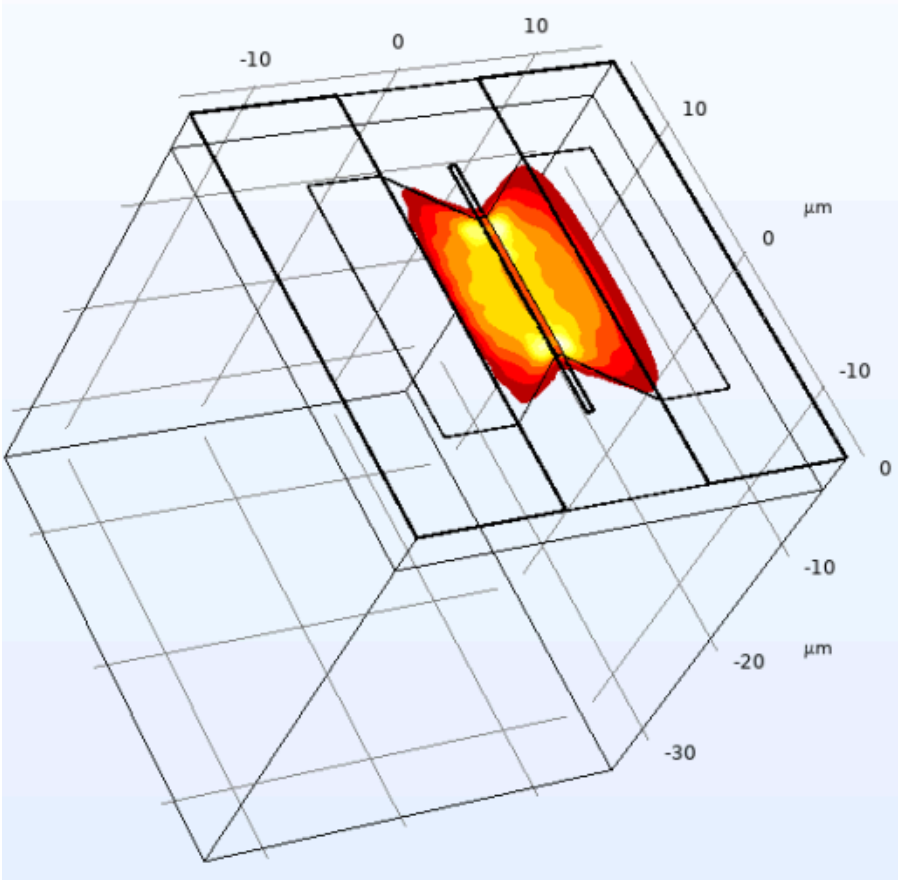
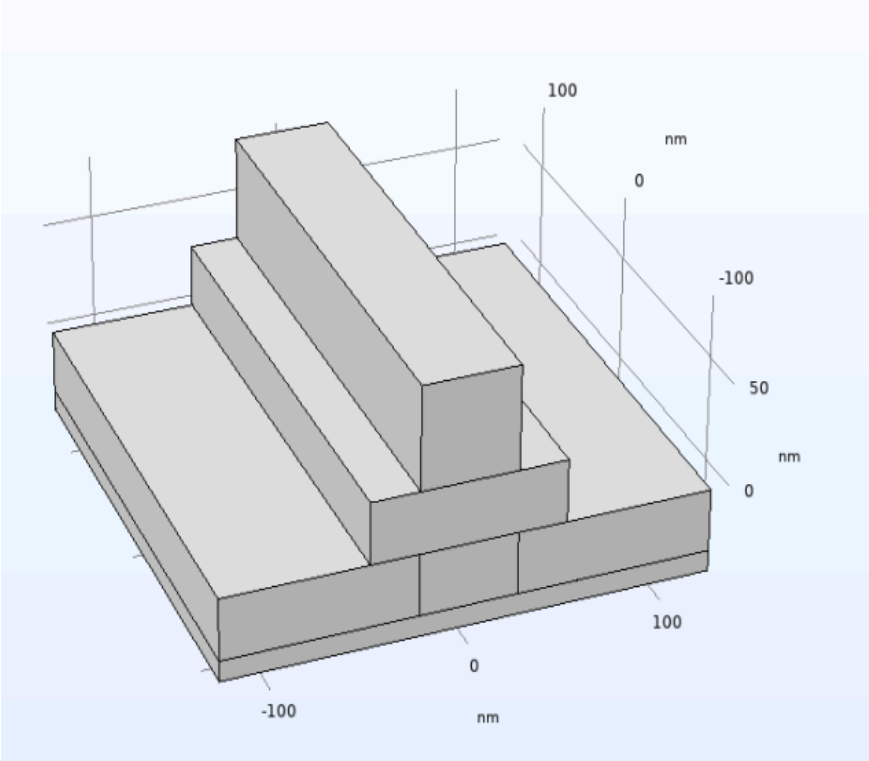


Fig. 2a.
This figure shows the heat dissipation that takes on the micro heater

Vertical Stack Memcapacitor



Sprint 2 Lowlights

1. Connecting different physical models using COMSOL proved difficult especially when considering the physics of each device.
2. Final Design not determined

Sprint 2 Summary

1. New shape was derived for the memcapacitor with a vertical stack
2. Simulated electrical physics for the device

Sprint 3

Goals:

During this project sprint, our primary objective is to enhance the geometry designs for both the Microheater and Memristor device, prioritizing considerations such as power efficiency, temperature limitations, and the effective functioning of electrical and heat components. Additionally, we aim to fabricate and rigorously test a physical system, including the tuning circuit, integrated with these devices. This comprehensive approach ensures that our efforts are geared towards optimizing performance while meeting all necessary criteria for functionality and reliability

Progress:

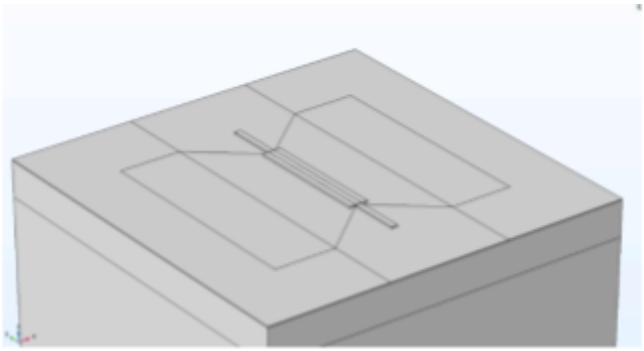


Fig. 3a.
Updated “lateral” design of memcap with microheater

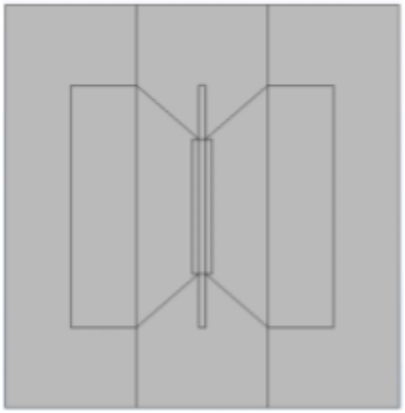


Fig. 3b.
Top view of combined heater and memcap device

The project sprint showcased notable achievements alongside some setbacks. Among the highlights, the updated designs of the memcap device, shown in fig. 3a and fig. 3b with the GST dielectric ‘sandwiched’ between metal contacts and placed above the microheater, successfully met the project's power objectives, marking a significant advancement. Furthermore, device simulations demonstrated satisfactory heat transfer to the phase change material (PCM), ensuring effective triggering of phase transition as observed in fig. 3c. However, the sprint also faced challenges, primarily stemming from delays in fabrication caused by scheduling issues with equipment. Despite these setbacks, the sprint overall demonstrated promising progress and potential for further development especially in regard to memory capabilities.

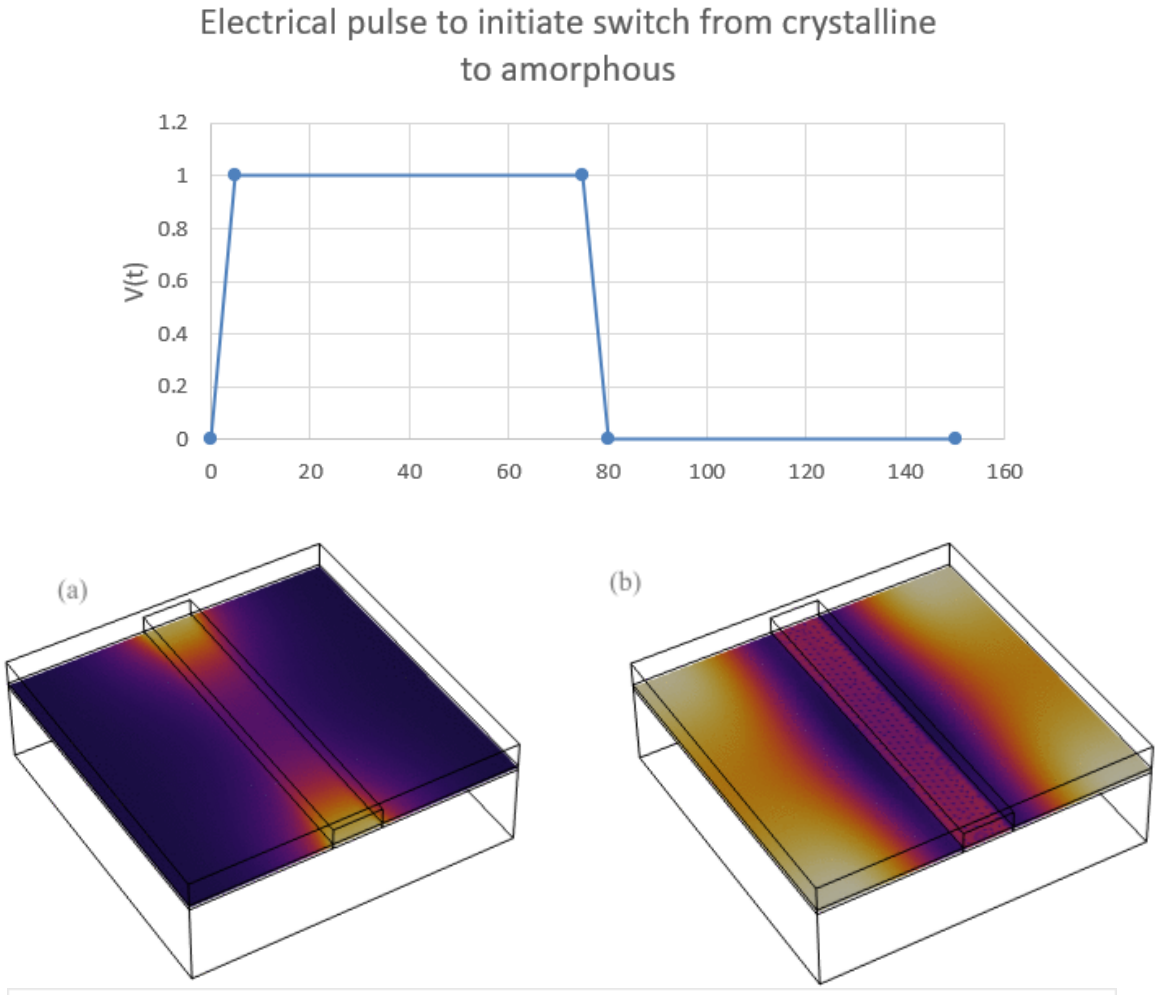


Fig. 3c.
(a) temperature increase in GST while amorphizing pulse is applied. (b) heat dissipation from the system while power is cut off

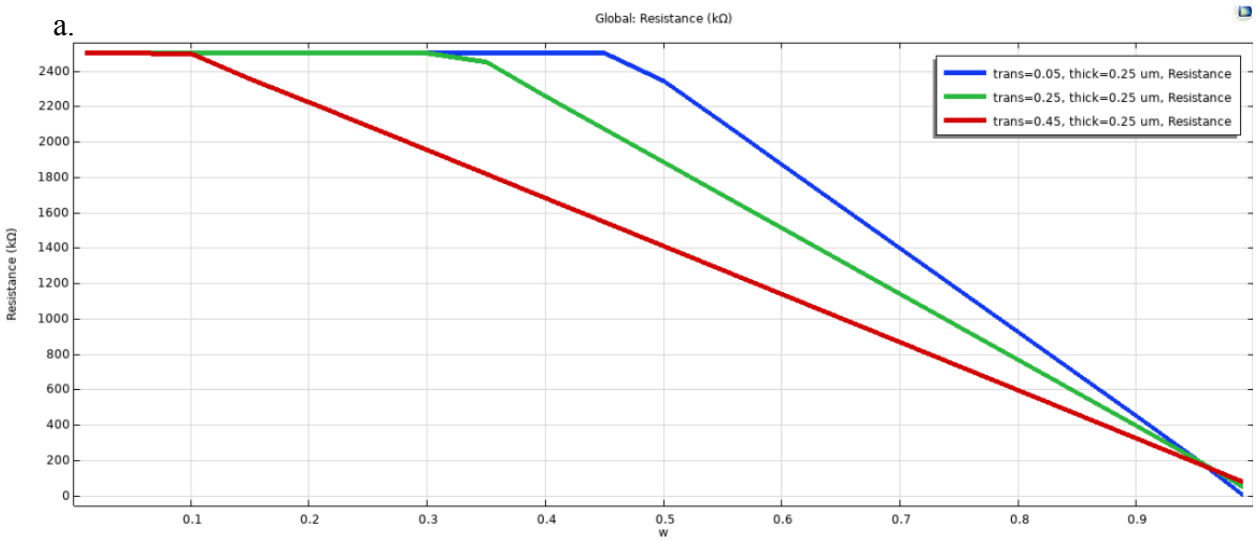
Results

Electrical Simulation

Inputs: Geometric model, Phase change distribution;

outputs: Capacitance, Resistance

a.



b.

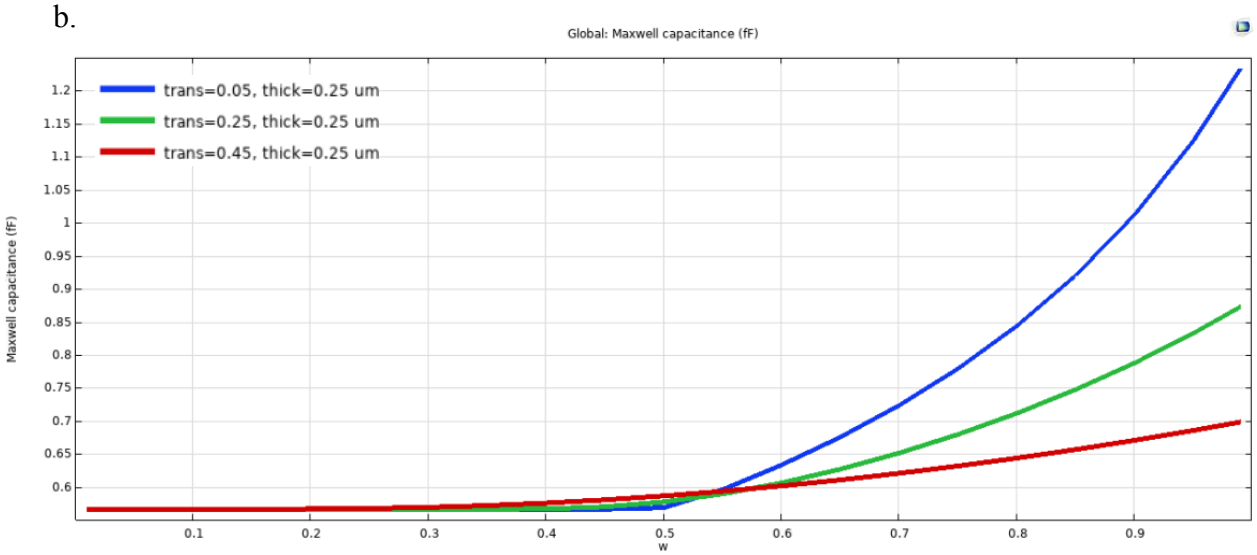


Fig. 4a.
(a) Normalized resistance vs crystalline PCM fill fraction (w), where w=1 implies nearly complete crystalline state. (b) Normalized capacitance versus w.
Assuming incomplete phase transitions, different colors (blue, green, red) correspond to different crystallinity distributions respectively

Heat Simulation

Inputs: Geometric Model, Voltage, Current; Outputs: Temperature Distribution (Max Temp. and Gradient)

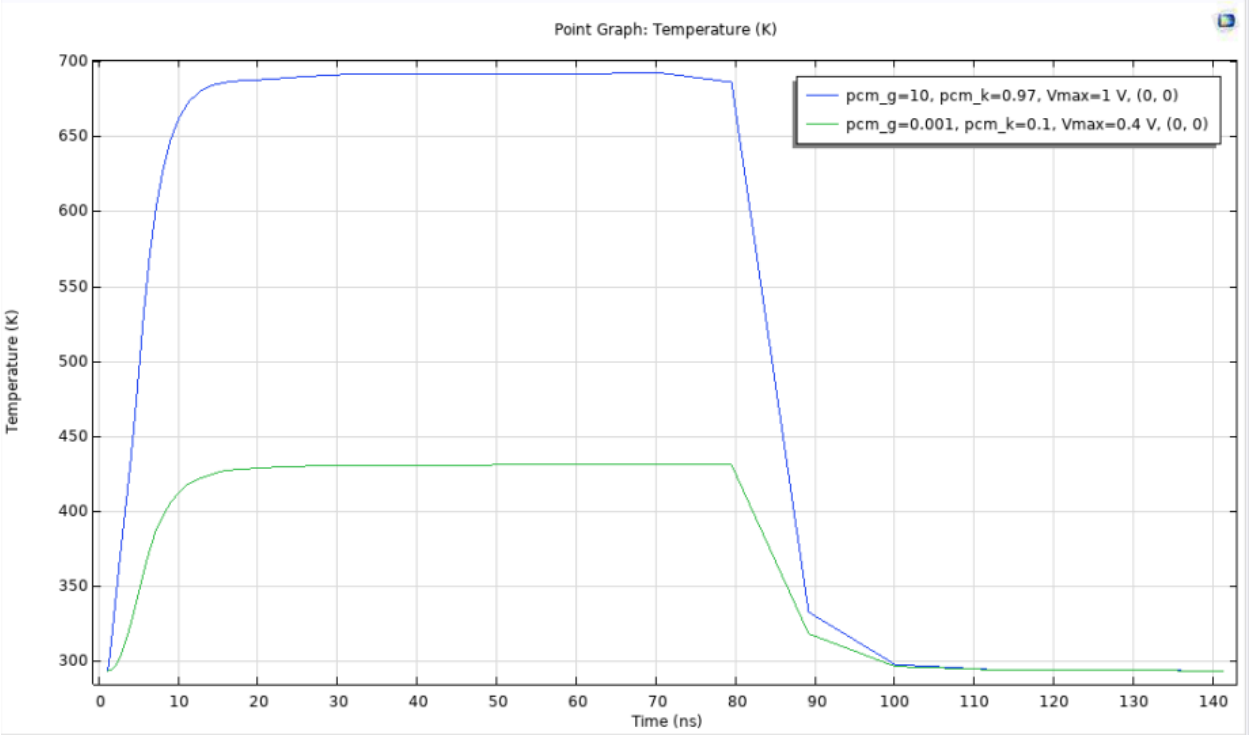


Fig. 4b.
Average temperature observed in GST dielectric when amorphizing pulse (1V) and crystallizing pulse (0.4V) are applied in different occasions

Conclusion

Conclusively, although we were not able to fabricate our device. We made significant progress in designing and simulating the geometry and physics of our phase change device. We understand that our device is beyond theoretical and is now achievable. Additionally, our device will have significant strides in modern computer logic and nano-technology .

References

M. Verdier, K. Termentzidis, D. Lacroix; Crystalline-amorphous silicon nano-composites: Nano-pores and nano-inclusions impact on the thermal conductivity. *J. Appl. Phys.* 7 May 2016; 119 (17): 175104. https://doi.org/10.1063/1.4948337

Wang, Lei & Wen, Jing & Yang, Cihui & Xiong, Bangshu. (2018). Potential of ITO thin film for electrical probe memory applications. Science and Technology of Advanced Materials. 19. 791-801. 10.1080/14686996.2018.1534072.

Z. Woods, J. Scoggin, A. Cywar, L. Adnane and A. Gokirmak, "Modeling of Phase-Change Memory: Nucleation, Growth, and Amorphization Dynamics During Set and Reset: Part II—Discrete Grains," in IEEE Transactions on Electron Devices, vol. 64, no. 11, pp. 4472-4478, Nov. 2017, doi: 10.1109/TED.2017.2745500.
keywords: {Grain boundaries;Computational modeling;Crystallization;Annealing;Phase change materials;Grain size;Amorphization;finite-element modeling;nucleation and growth;phase-change memory (PCM);set and reset},