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Senior Design Final Solution Report

POWER INTEGRITY EVALUATION SYSTEM

EECE 401 & 404: Senior Design 2024-2025

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Summary:

Power Delivery Network (PDN) is the infrastructure within a circuit responsible for supplying power to all the components in the circuit. Ideally, it is supposed to supply a constant voltage. However, as the modern electronics and high frequency circuits strive toward increasing computational performance and minimizing power consumption, the noise in the PDN becomes more prominent and could lead to malfunctioning of the whole system. In the industry, each major electronics company has huge teams working to mitigate such issues on their product. Still, undergraduate curriculum and its graduates understand the PDN to be "ideal", having no understanding of its behavior. Our capstone project addresses this gap with a cost-effective power integrity evaluation toolkit that facilitates a case study of a PDN prototype to provide hands-on experience and understanding of this problem, as well as skills required to work and mitigate similar problems.

Our product, at this stage, consists of printed-circuit-boards (PCB) of a ring oscillator circuit with control and test points and another board with transmission line test structures as well as all the component required for their bring-up. On a time domain characterization, the users can observe the signal propagation of the ring oscillator as well as the voltage fluctuations in the PDN using an oscilloscope. Whereas, using a vector network analyzer (VNA) will enrich their grasp on transmission line behavior in frequency domain and how that accounts for the noise in the PDN. In our demonstration, we also expanded our solution to look into the PDN of an FPGA board, which we will incorporate with a custom PCB in the future.

Through this report, we discuss the constraints and design choices for our toolkit as an electronic product, justifying the reasoning for our decisions. Then, we walkthrough the development of the toolkit from circuit design, circuit and electromagnetic simulation, breadboarding, PCB design and bring up to conducting test, recording measurements, and problem evaluation. We delve deeper into the need for this product in an university setting to undergraduate students, and the perspective it brings to the user students on their future work.

Problem Statement:

Understanding the importance of Power Delivery Network (PDN) Noise, a growing issue in modern electronics, becomes increasingly crucial as electronics continue to advance, despite its limited coverage in undergraduate-level curricula. Our approach is to design a power delivery network for widely used candidate circuits and observe and evaluate the noise in the PDN. Our design ensures proper identification and evaluation of Power Delivery Network noise within the specific circuit, thereby aiding in the development of an understanding of this issue and the skills required to work with and mitigate similar problems. Our product is a cost-effective and beginner-friendly product for an already niche market and expensive alternatives.

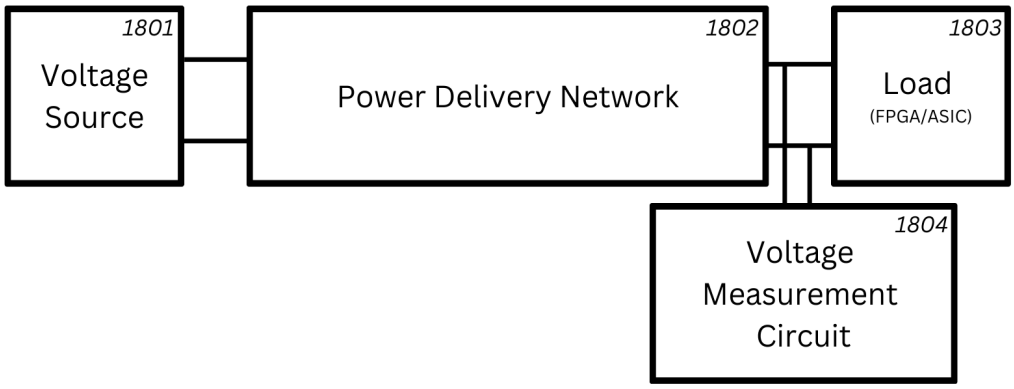
Design Requirement:

Requirements	Items	Quantity
Product Specification	**Inputs:**	max 5V Supply
	Dimensions:	max (100mm*100mm)
	Operating limit:	10MHz-10GHz
	Weight:	0.6 lbs
	Platform/Hardware:	1) Custom Printed Circuit Board (PCB) for a Ring Oscillator Circuit 2) CMOD S7 Field Programmable Gate Array (FPGA)
Constraints	**Environmental Constraints**	• PCB will be made partially of copper as it can be reused even when the device has stopped operating. • PCBs are free from hazardous materials, making them safer for consumers and reducing environmental contamination (RoHS)
	Socio-cultural Constraints	• Documentation for users to be available in various languages to account for different cultures and backgrounds • PCBs will be color-coded by considering the market requirements and user needs. For eg: Apple prefers black-colored PCBs.
	Compliance (Rules, Regulations, and Standards)	• Electromagnetic Compatibility Compliance (EMC) • Underwriters Laboratory Certification • RoHS Compliance (Restriction of Hazardous Substances Directive)

Solution Design:

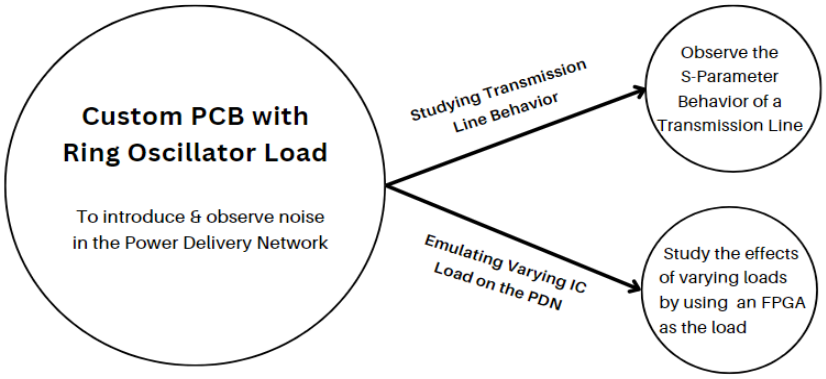
For the solution design, the system was divided into four parts. The parts are described in the block diagram below:

Block Diagram



The transmission of power through the Power Distribution Network (PDN) **1802** from voltage source **1801** to load **1803** experiences voltage fluctuations in high-frequency circuits disabling the circuit from proper operation. The voltage measurement circuit **1804** is the available instrument in the lab that will help us look at the signals and compare them with the noise in the PDN. The instruments are probed on the pads of our PCB layout placed right before load **1803**.

As an initial design, a simple ring oscillator was chosen as the Load **1803** due to its wide-spread use in modern electronics. The product was tested through comparisons with simulations and measurements of the board itself.



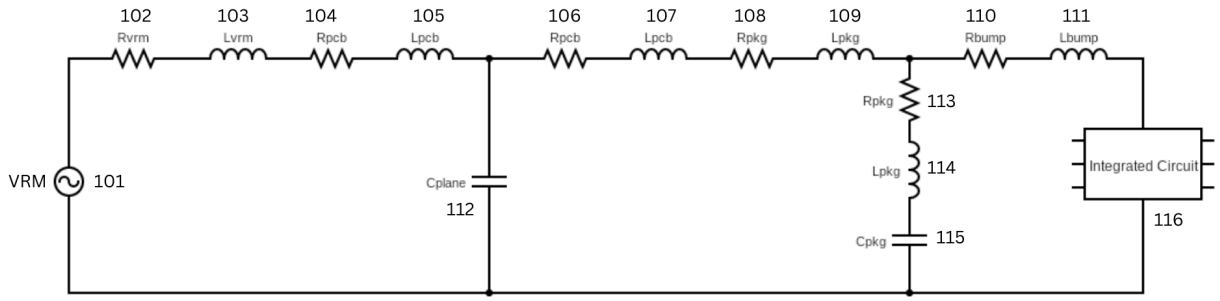
Our custom PCB with ring oscillators as load is the initial design for the power integrity evaluation system. The solution design then expands to incorporate the study of transmission line using another custom PCB with transmission line test structures to understand the insertion and return of a signal as its transmitted through the PDN path. Also, we expand to FPGA to emulate different circuits to understand how different varying loads with more complex structure have different impacts on the PDN noise.

To make the design feasible for the initial and advanced development each of the blocks was reiterated and adjusted to find the final solution. The top solution design for each block is described below:

Voltage Source **1801**: Two sources have been used:

- 5V AA battery Source to supply voltage to custom-designed PCB.
- 5V supplied from laptops to supply power to, and program the FPGA.

Power Delivery Network(**1802**): The First Order Lumped Element Model was used to represent the Power Delivery Network.



According to the diagram, the circuit represents a PCB in which the Voltage Regulator Model(**VRM, 101)** helps us supply a constant voltage to the Integrated Circuit(**IC, 116),** using a two-port network. The parasitics for each part of the network are modeled, the VRM(**101)**, the transmission line(**104-107)**, the package(**108-109,113-115),** and the connection(**110-111)**. In this design, we have included the Parasitic Inductance within VRM(**Rvrm+Lvrm, 102,103**). Then we also have the Parasitic Capacitance modeled for the two planes(**Cplane, 112)**. Then, we modeled the Inductance and the Resistance in the transmission line (**Rpcb+Lpcb, 104-107**). We also added the R and L noise in the Package (**Lpkg+Rpkg, 108-109,113-115**). Finally, we added the parasitics in the connection bump(**Rbump +Lbump,110-111**). This schematic considers the constraints presented in an actual PCB which helps us simulate the PDN noise accurately.

Voltage Measurement Circuit **1804:** Testing pads to assist different lab-available equipment are added to the PCB. Some of the readily available voltage measurement circuits used are:

- Multimeter: To measure the signal and intensity.
- Analog Discovery Kit: To measure the signal and intensity.
- Oscilloscope: To measure the signal and intensity.
- Vector Network Analyzers: To look at the S-parameters

Load **1803**: The Load is a ring oscillator as it is a very widely used circuit in modern electronic systems for its role in clock generation, digital signal processing, and low-power applications. The switching of not gates would create workload fluctuations which would add voltage droop to the PDN, which if not addressed through our bulk and decoupling capacitors, could lead to noise in the Power Distribution Network.

Project Implementation:

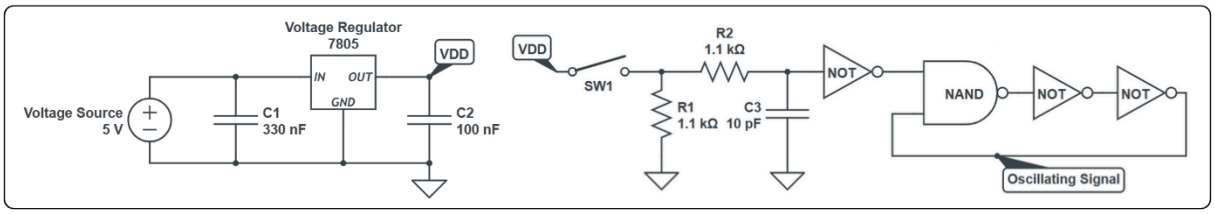
Using the agile model for solution implementation we were able to successfully achieve our expected deliverables. Below you will find our agile workflow and weekly plan:

Starting Date of Week (M)	Sprint #	Increment (or intermediate working component)	Weekly development tasks
1/30/2024	1	Fabricate the base implementation for the PDN with Ring Oscillator as the load.	Work on simulations(LTSPICE, ANSYS) & layout(KiCAD)
2/5/2024			Complete the simulations and send for fabrication
2/12/2024			Breadboarding/PCB Bringup & Testing
2/19/2024	2	Build another version to better demonstrate the problem in discussion with an FPGA/microcontroller acting for the varying load.	Finalize the circuit schematic & computing functions
2/26/2024			Work on the simulations - LTSPICE and Ansys
3/4/2024			Spring break
3/11/2024			Complete and compare simulations & breadboarding
3/18/2024	3	Fabricate, test and fine-tune the system built in the second phase.	Finish the new layout and send for fabrication
3/25/2024			FPGA/Microcontroller testing & PCB Bringup
4/1/2024			PCB finetuning, testing, and comparison

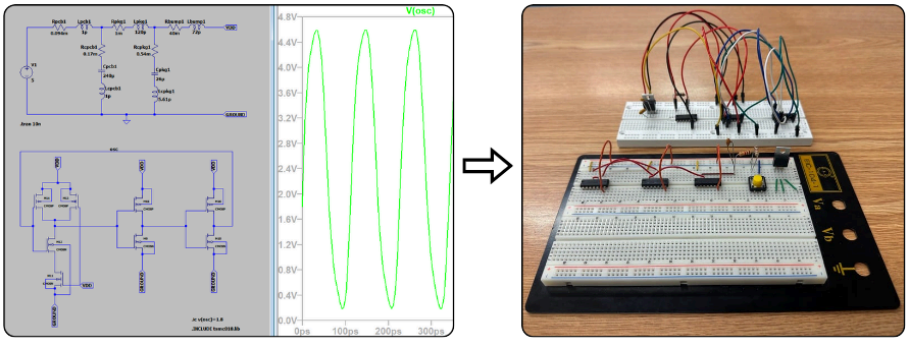
Project Implementation Process:

#Sprint 1

Our work started with defining the architecture for the ring oscillator, where our design consists of a three-stage ring oscillator with two NOT gates and one NAND gate. The NAND gate acts as a NOT when one of its inputs is tied to VDD and a buffer when it's tied to the ground, making the whole circuit either a ring oscillator or a buffer. The circuitry before the NAND gate comprises of a switch button to control that input to either be a ground or VDD. On the other hand, we designed for a 5V battery source and the 7805 voltage regulator.



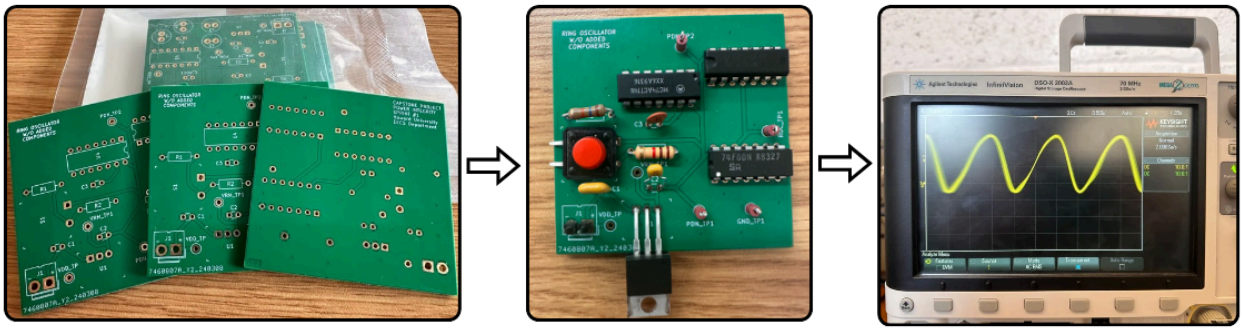
Next, we took the design into LTSpice for circuit simulation and observed the oscillating signal as output and verified the functionality of our design. Then, we breadboarded our circuit using 7400 series of transistor-transistor logic (TTL) integrated circuits (7400, 7404, 7414). After then, we probed our breadboard circuit to observe the same oscillating signal to verify functionality and also, the noise in its power delivery network. We will evaluate the results after the discussion of the implementation process.



Within the first sprint, we also took our design to KiCAD to design a PCB layout of our ring oscillator circuit.

#Sprint 2

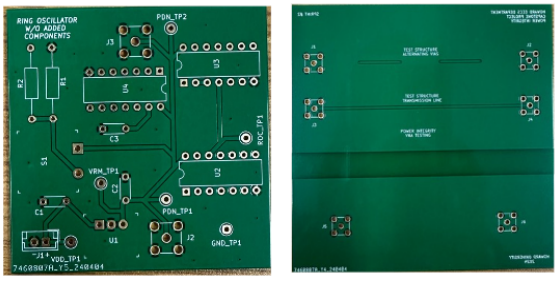
This sprint started with improving the PCB design by adding test points as well as replacing the component footprints and rerouting the traces. We then sent our PCB design for fabrication. While waiting for the PCBs to get back, we focused on electromagnetic wave simulation in Ansys HFSS. We figured that frequency domain characterization would be an important aspect in our project, as such we began our investigation of S-Parameters. We designed different transmission line structures as microstrip line, coplanar wave guide, and coplanar wave guide with meandering vias in Ansys HFSS, to observe the insertion and return loss in frequency domain.



As our fabricated PCB got delivered, we soldered all the components and brought it up. Then, similarly, we conducted oscilloscope tests and recorded the values.

#Sprint 3

On the last sprint, our focus was to conduct vector network analyzer tests, and also expand our evaluation into an FPGA board. For VNA tests, we added SMA connectors to our ring oscillator PCB design, as well as designed another PCB layout that consists of the different transmission line structures from the second sprint. As these two PCB boards

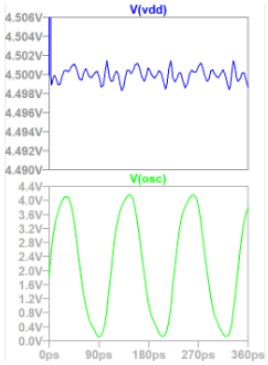
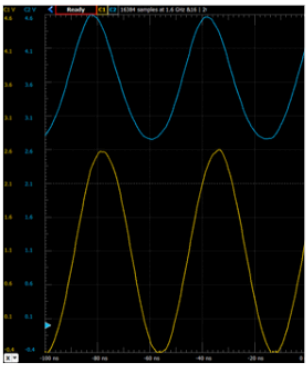
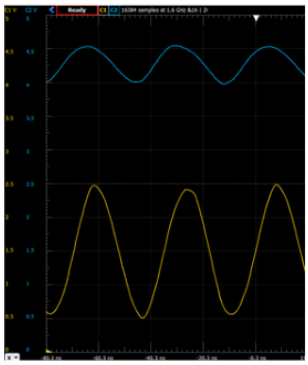


came back from fabrication, we soldered and brought up the board. Then, we used the Nano VNA H4 to take and record the S-Parameter measurements.

On the other hand, we took the CMOD S7 FPGA to implement a frequency-based LED blinking system to probe and evaluate the PDN of the FPGA.

#Observation & Evaluation

As discussed before, our evaluation focuses on time domain characterization, to ensure correct operation and signal propagation, as well as frequency domain characterization, to observe the transmission line behavior in high frequency scenario.

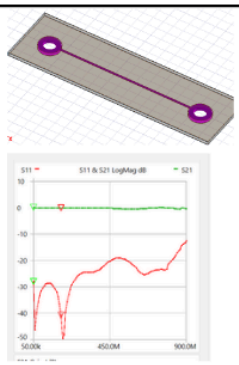
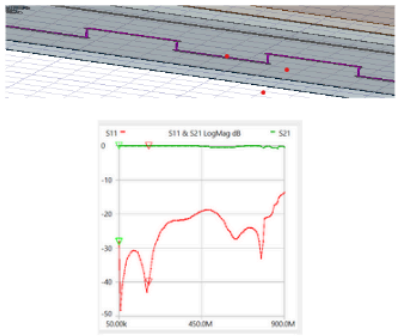
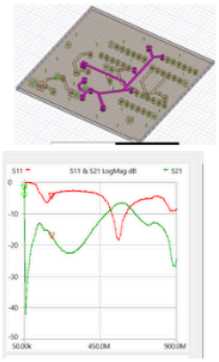
Circuit Simulation: LTSpice	Breadboard Measurement	PCB Measurement
		
Pk-Pk Voltage: 4.1 V Frequency: 9.4 GHZ	Pk-Pk Voltage: 3.1 V Frequency: 28.3 MHz	Pk-Pk Voltage: 2V Frequency: 37.2 MHz
Pk-Pk Voltage: 1mV	Pk-Pk Voltage: 0.6V - 1.8V	Pk-Pk Voltage: 0.3 V - 0.6V

The table above shows the noise in the PDN as the blue signal, and the oscillating output as the green or orange signal on simulation, breadboard, and PCB measurements. As we can observe, the general trend on both the signal are very similar. Looking at the oscillating output signal, we can the peak-to-peak voltage varies from 4.1 V in simulation, 3.1 V in breadboard, and 2V in the PCB. This variation is generally characterized by the added parasitics, however, all these signals verify us that the ring oscillator is functioning.

However, looking at the noise in the PDN, we see that the circuit simulation only observes a 1mV peak-to-peak voltage. This observation with the first order lumped element model of the parasitics in the PDN depicts that circuit simulation still doesn't account much of the electromagnetics issues and underlying physics in the circuit. Because as we can observe in the breadboard and PCB implementations, the peak-to-peak voltage for the noise shows to be 0.6 V - 1.8 V or 0.3 V - 0.6 V in a 5V power supply. This implicates the power integrity issue we are trying to explore and aware the undergraduate students about. This evaluation is necessary

because if such issues are not addressed in advanced systems, it could easily lead to malfunctioning of the whole system.

To evaluate this underlying physics of the problem, we then look into S-Parameters of the PDN line to understand its behavior and observe how power integrity becomes more crucial in higher frequency.

Simple Transmission Line	Multi-via transmission line	Ring Oscillator Circuit
		
Simple Transmission Line: Frequency 500kHz-900MHz	Multi-via transmission line Frequency: 500kHz-900MHz	Ring Oscillator Frequency: 500kHz-900MHz
S11 return loss: -40.716dB S21 insertion loss: -28.035	S11 return loss: -40.088dB S21 insertion loss: -28.224dB	S11 return loss: -4.463dB S21 insertion loss: -4.305dB

Our learning kit is designed to give students a hands-on opportunity to examine various PDN configurations and assess their impact on signal transmission. Displayed above are our efforts to investigate signal transmission across different PDN designs, which include: a simple transmission line, a transmission line with alternating vias, and a ring oscillator circuit. Our approach involves obtaining S-parameter measurements for PCB-layout circuits via Ansys simulation software and corroborating these measurements with data from the actual PCBs tested using a Vector Network Analyzer (VNA).

Additionally, another part of the learning kit we developed during the course was a Machine Learning Model capable of predicting S-parameters given different features of the PCB like board thickness, length and width. This was developed using a feedforward neural network which was trained from thousands of varying data points. We believe this software package will enhance the overall learning process for students as they will see firsthand what factors influence scattering parameters and how PCB design is shaped by this.

#Project Expansion - FPGA Implementation:

To meet our customers' needs, who are university students, we wanted to make the system feasible for any kind of load circuit. This is possible through the use of a Field Programmable Gate Array (FPGA), where different kinds of circuits can be emulated by programming. For our design, we could not fabricate a PCB with FPGA but were able to evaluate the noise in the

power delivery network in an FPGA board readily available in the market, CMOD S7. The noise was observed in a power delivery path, from the FPGA to the LED, where the frequency for the clock was 12 MHz and the frequency for the blinking LED was 10 HZ. We observed that the PDN had a noise equivalent to 35.75mV, which is not significant and is a result of the use of the bulk and decoupling capacitors as the mitigation technique for the noise in the Power Delivery Network.

Fig: CMOD S7 FPGA

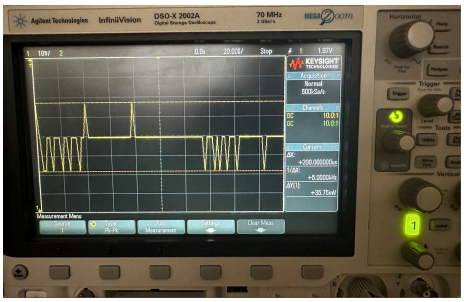


Fig: 37.75mV pk-pk Noise in the PDN

Conclusion:

At the end of our senior design project, we successfully built a product to observe noise in the form of voltage fluctuations in a variety of different circuits. These observations meant undergraduate students could have a better understanding of the behavior inside a transmission line and better explore the topic of power noise. Insights revealed to us include the understanding that a PDN does not have DC-DC connectivity and that the PDN has built-in parasitics and underlying physics that contribute to the noise production in the circuit.

In completing this project, we were faced with numerous challenges. One challenge included the limited capabilities of the Ansys student version. We had limitations on the size mesh we could use in our simulations. This was less than the planned size of our PCBs and as a result we had to adapt our test designs to meet the requirements of the software. There was also an inability to import s-parameters onto LTspice which was the circuit simulation software we used. We intended to observe the Ldi/dt phenomenon on a simulation software and compare these to the actual PCB that we fabricated. However, due to this challenge, we were unable to explore further in this aspect.

Another challenge was that we underestimated the amount of time required for testing and measurement of our fabricated devices. We had designated specific periods of time during a sprint for testing specifically but it had taken more time than accounted for and we had to include it in the next sprint thus leading to less time available to focus on some of our intended plans.

However, despite these challenges, the project was an overall success regarding skills gained and confidence we developed as engineers. Concerning the new skills the team gained, we had hands-on experience simulating, modeling, and designing PCBs. The team also gained experience with measurement devices like oscilloscopes and VNAs. Additionally, many

opportunities arose to read many different academic papers to broaden our perspective on the problem at hand.

In the future, we hope to incorporate and explore noise mitigation techniques, and utilize machine learning to build optimal PCB circuits that minimize noise interference and transmission loss. Furthermore, we want to customize our PCBs using FPGAs to analyze a wide range of more complex circuits.

References:

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